Recent Trend of NVM Technologies

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Agenda

- Introduction
- Transistor Based Memory Scaling
- No Transistor Memories
- Non Litho Defined Memories
- Summary

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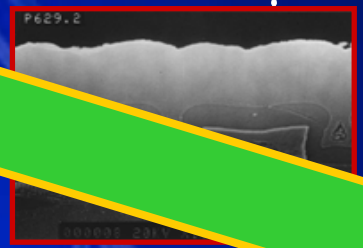
Introduction

- Moore's Law Continues
- Recent work on NOR and NAND memory scaling showed promising research ideas for 45 and 32 nm nodes
  - NOR and NAND will be the high volume production flash memories for the rest of this decade
- Innovative research work continues to look for alternatives: continuation of Moore's Law for the long term or go beyond Moore's Law

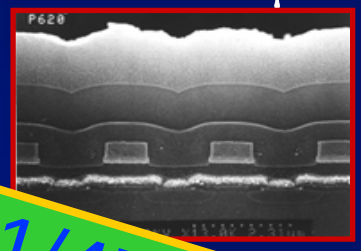
Intel ETOX® (NOR) Technology Scaling

1986 / 1.5µm

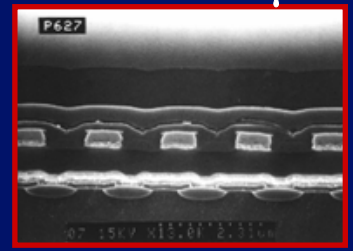
1988 / 1.0µm



1991 / 0.8µm



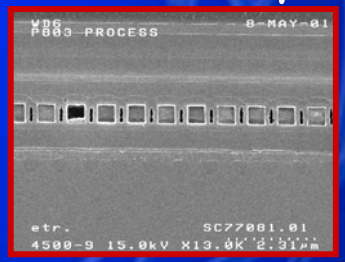
1993 / 0.6µm



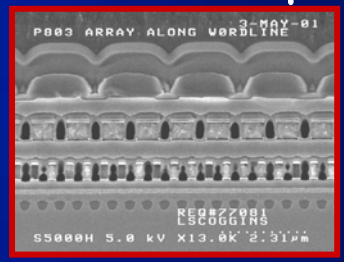
1996 / 0.4µm

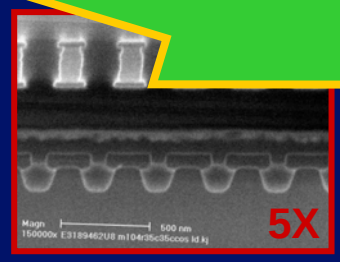
1/476

1998 / 0.25µm

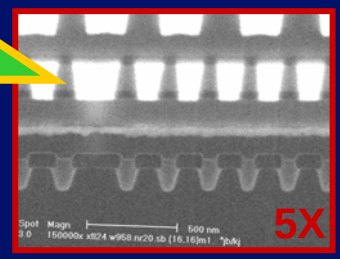


2000 / 0.18µm





2004 / 90nm

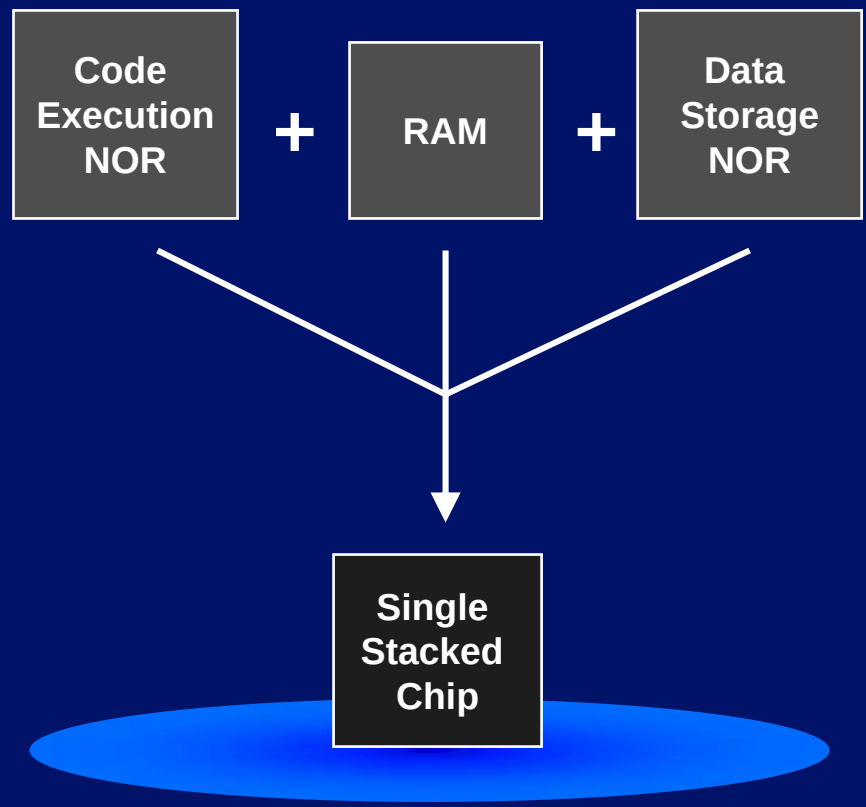


Volume Production Year / Technology Generation

- 16+ years & 8 Generations of ETOX® (Intel NOR) High Volume Production to 0.13 µm
- 5+ years and 4 Generations of Intel StrataFlash™ (Multi Level Cells 2bit / cell) memory

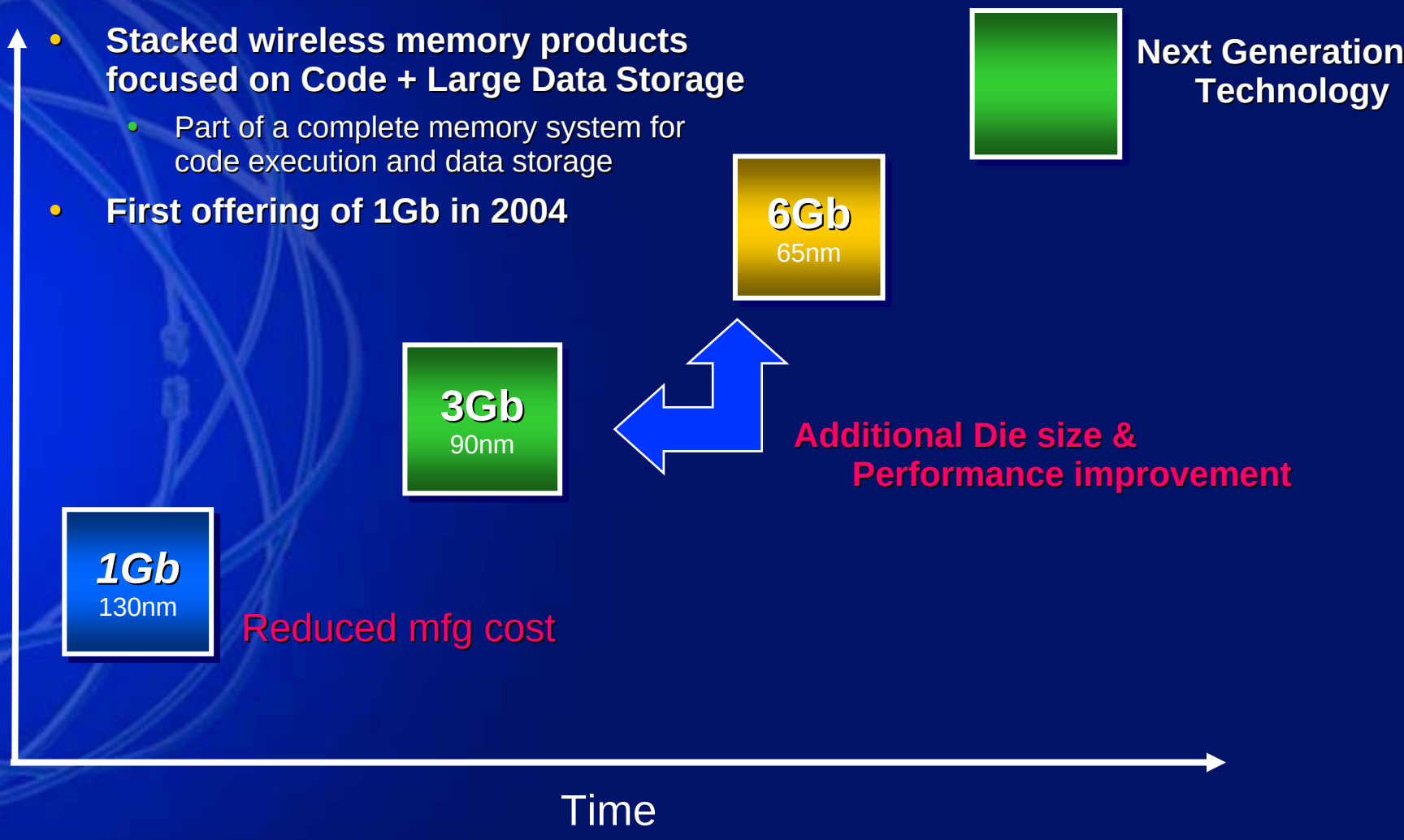
NOR memory solution for code and large embedded data

- **Complete memory system solution**
- **Flexible solutions for code plus large embedded data up to 1Gb**
- **MLC technology optimized for data storage delivers a very cost effective solution**



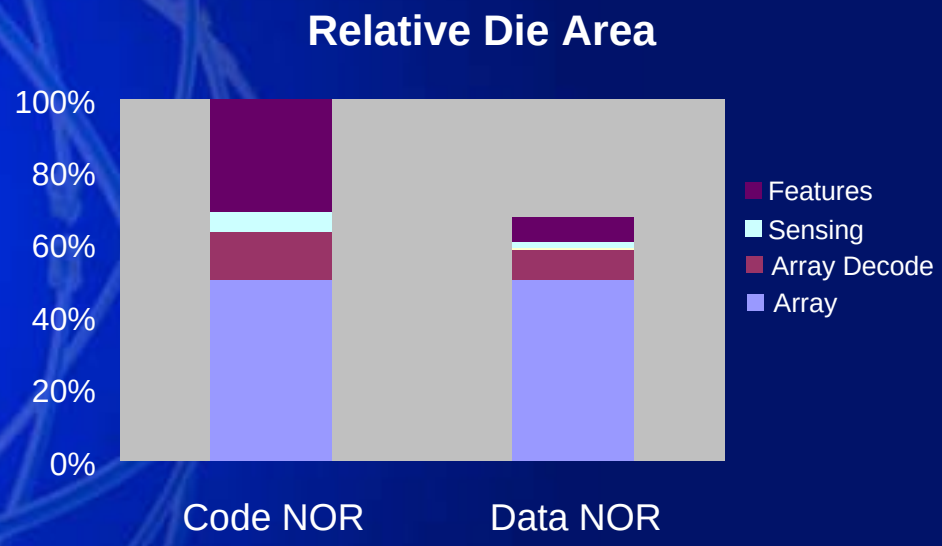
Intel Flash® Memory for Code + Data

- **Stacked wireless memory products focused on Code + Large Data Storage**
  - Part of a complete memory system for code execution and data storage
- **First offering of 1Gb in 2004**



Data Focused NOR Technology

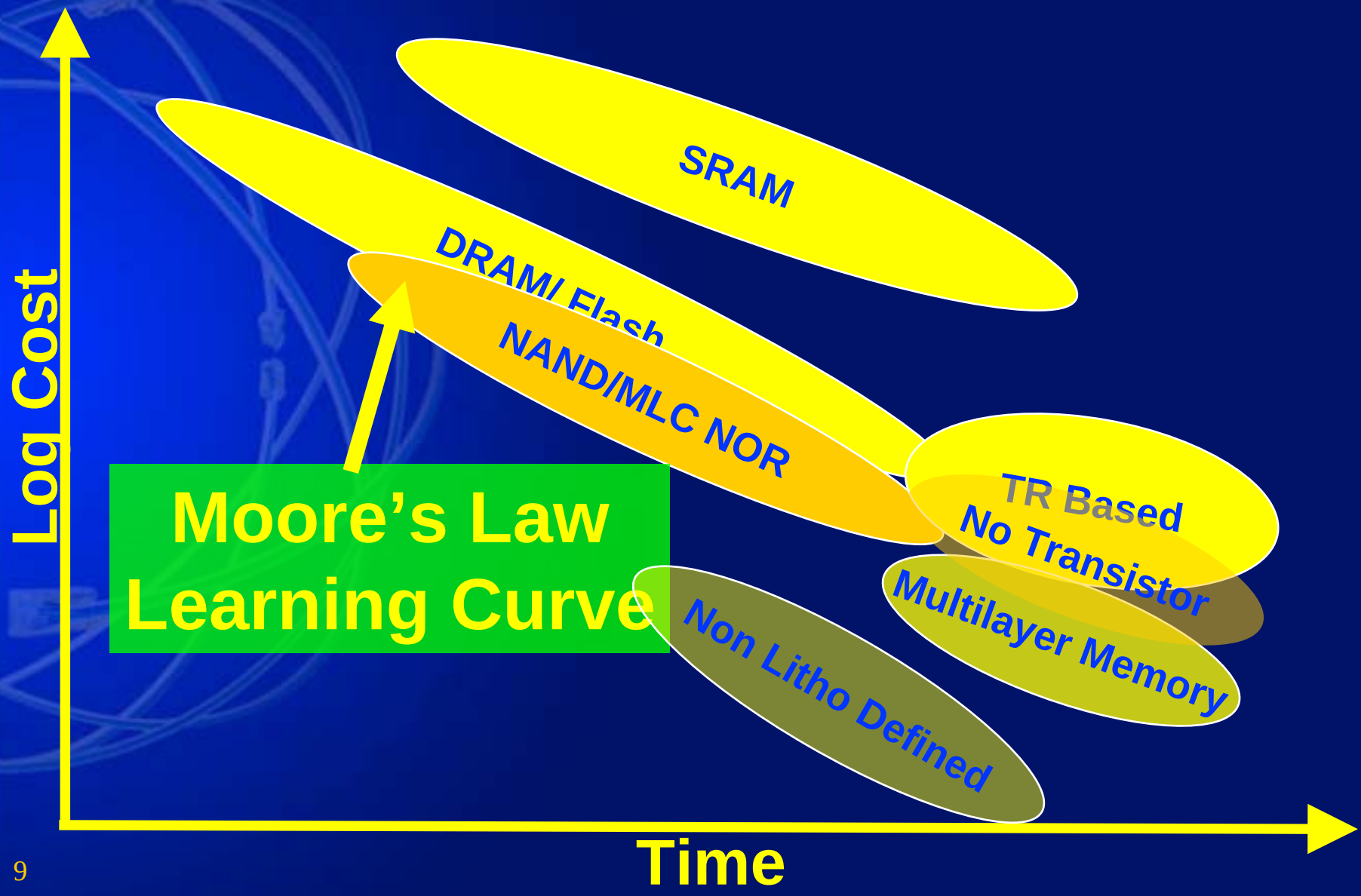
- **Feature Reduction Impact on Die Size**
  - **Removing XIP Focused Features Results in Approximately a 30% Reduction in Die Size**



XIP Features :
- Read While Write
- High Performance Read
- Parameter Block
- Block Locking

- **Feature Reduction Impact on Technology**
  - **Removing Performance Focused Features Results in Approximately a 10% Reduction in Wafer Cost**

Memory Cost Projection



Summary of Memory Cost Projection

- Memory with transistor first to slow down (beyond 32 nm node?)
- Memories without memory transistor limitation can continue scaling
- Multilayer memory can give one time cost reduction but stays on Moore's Law
- Non litho defined memories can go beyond Moore's Law

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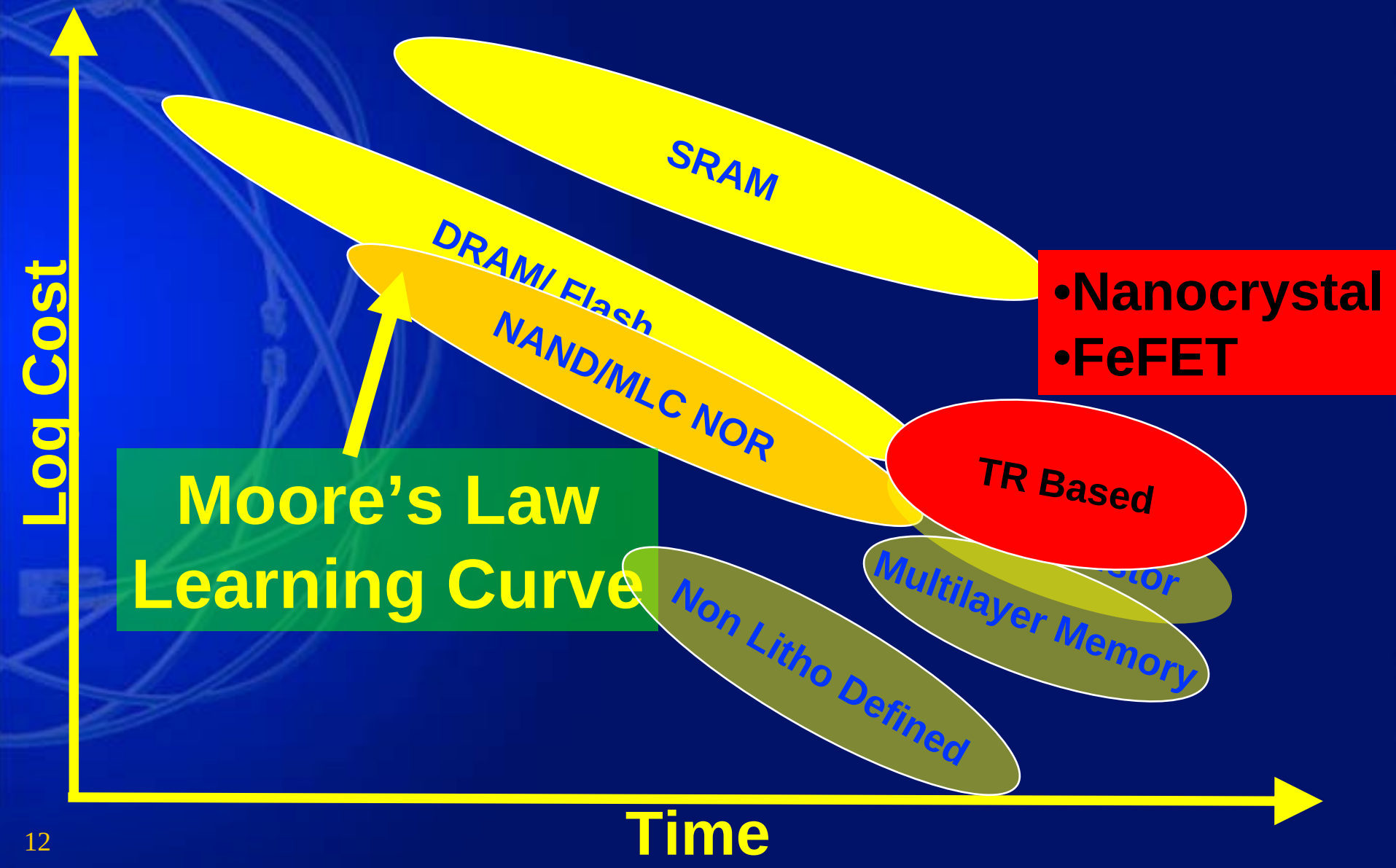
Memory Cost Projection



Nanocrystal Memory

Nanocrystal

- Nanocrystal technologies were proposed to extend floating gate scaling
- More applicable to NAND scaling with channel tunnel and erase
- Innovation reported:
  - Back floating gate
  - Self assembled
  - Improved tunnel barrier
  - Metal Islands (single and double layers)

One View of flash scaling

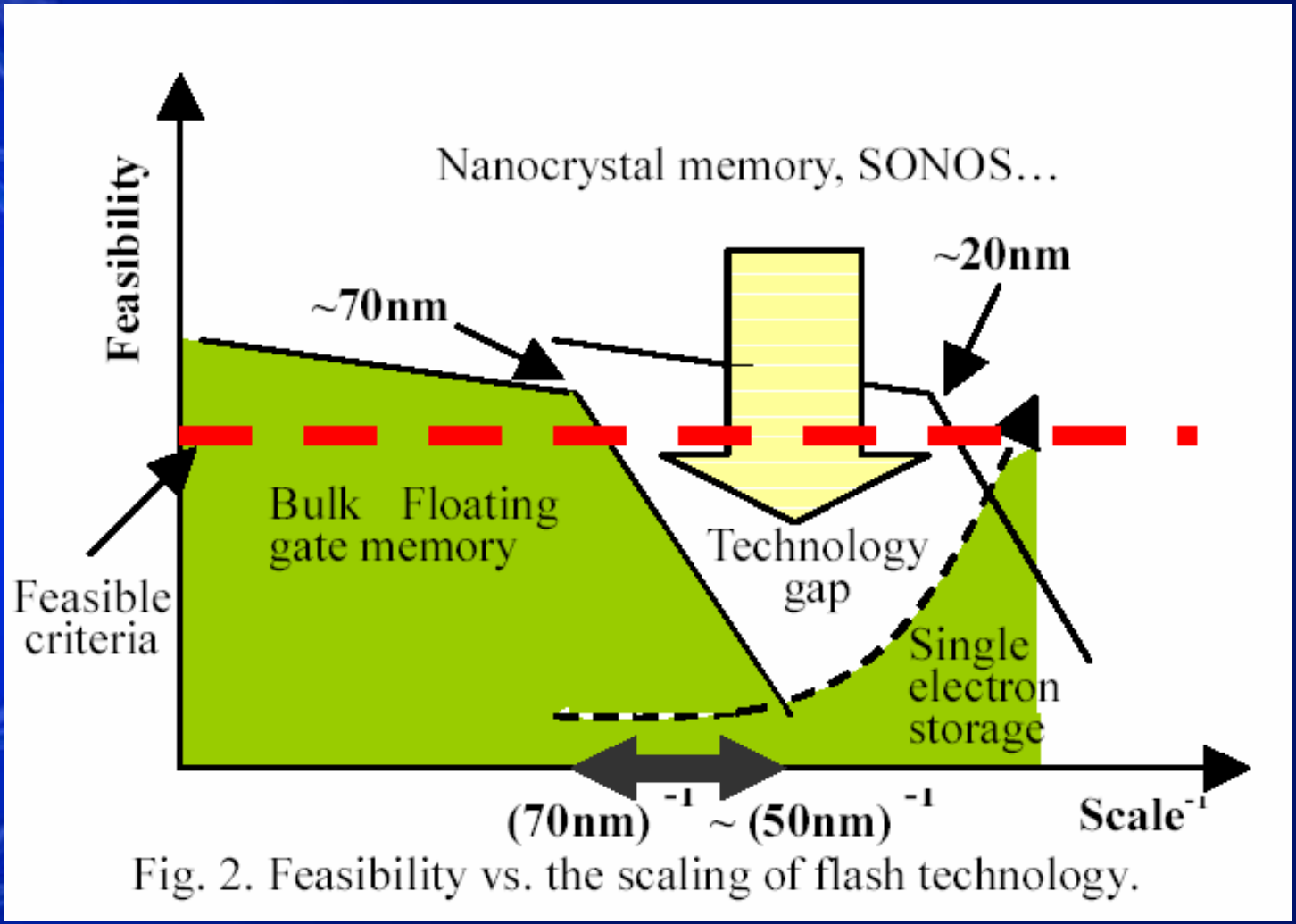


Fig. 2. Feasibility vs. the scaling of flash technology.

"High Speed and Nonvolatile Si Nanocrystal Memory for Scaled Flash Technology using Highly Field-Sensitive Tunnel Barrier", S.J. Baik et al., 2003 IEDM Technical Digest, Session 22.3.

Silicon Nanocrystal

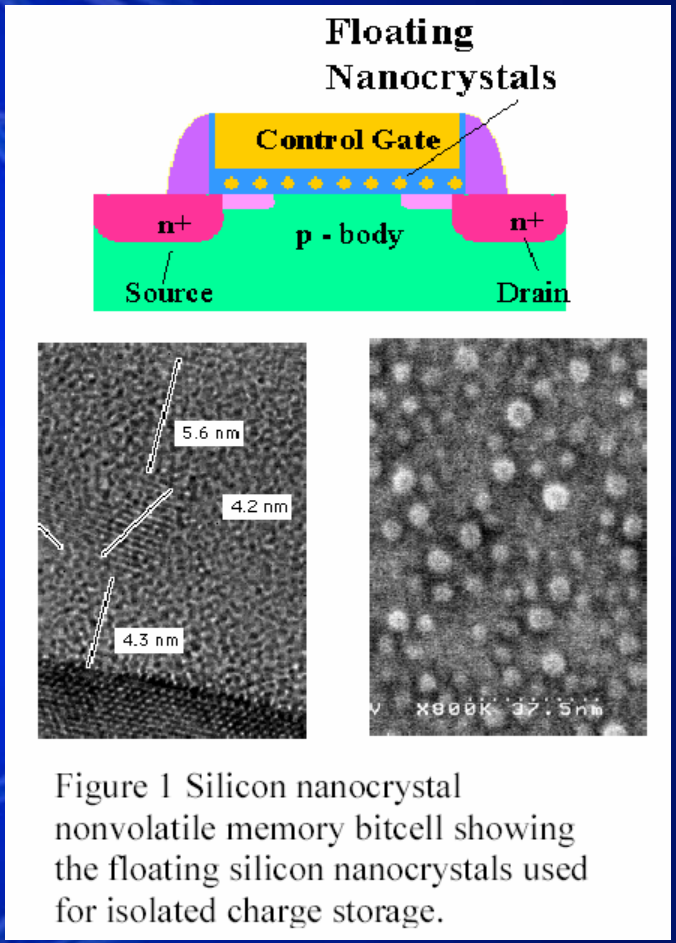
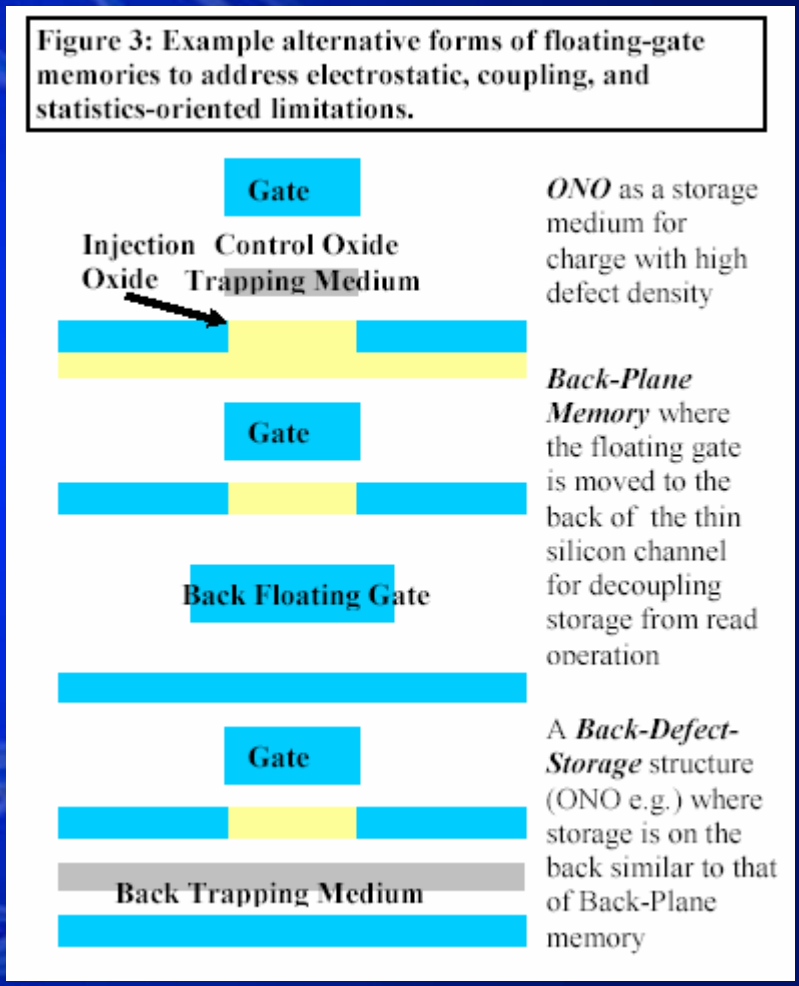


Figure 1 Silicon nanocrystal nonvolatile memory bitcell showing the floating silicon nanocrystals used for isolated charge storage.

"A 6V Embedded 90nm Silicon Nanocrystal Nonvolatile Memory", R. Muralidhar et al., 2003 IEDM Technical Digest, Session 26.2.

- Instead of charge stored in floating gate, charge is stored in nanocrystals
  - Similar to nitride storage but better control
  - Reduce floating gate coupling
  - Reduce SILC effect
  - Process simplification

Alternative Cell Structures



"Few Electron Memories: Finding the Compromise Between Performance, Variability, and Manufacturability at the Nano-Scale", S. Tiwari et al., 2003 IEDM Technical Digest, Session 10.5.

- Instead of front side charge storage, back side can also be used
  - Either floating gate or floating traps (nitride or nanocrystals)

Nanocrystal fabrication by Polymer self Assembly

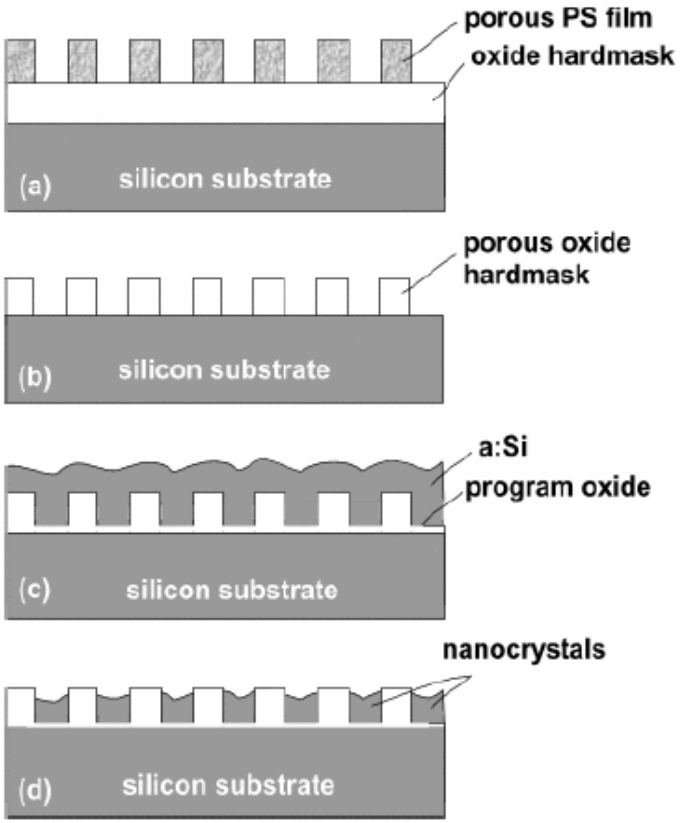


Fig. 1. (a-d) Schematic diagrams of the process flow used to create an array of Si nanocrystals beginning with a porous self assembled polymer template.

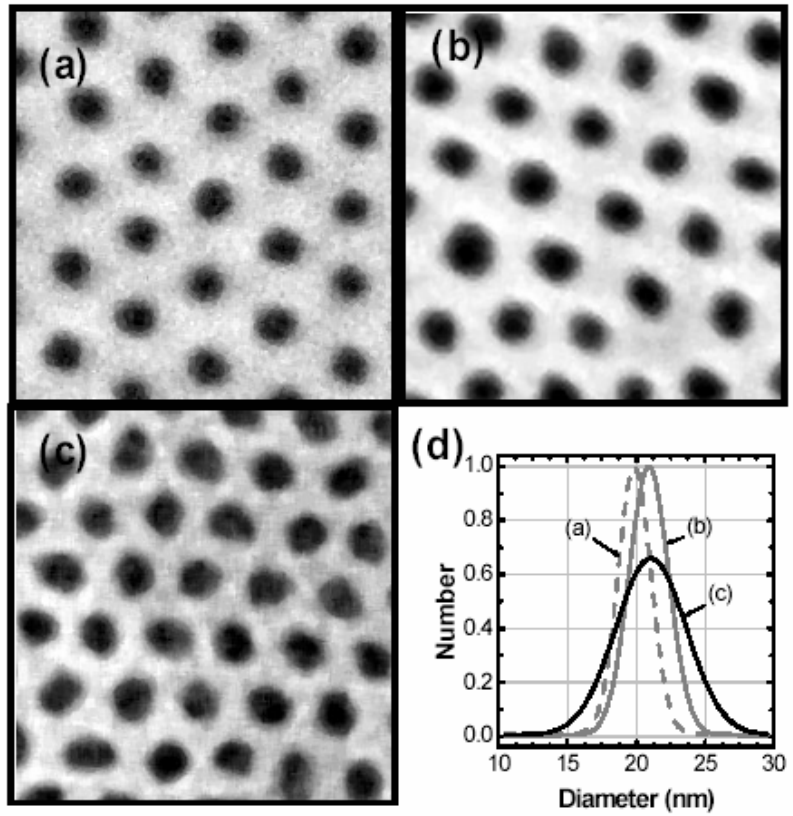


Fig. 2 (a-c) 200×200 nm top-down SEM images of (a) porous polymer film on SiO_2, (b) porous dielectric after pattern transfer into the SiO_2, and (c) Si nanocrystal array. (d) Distribution of polymer pore, dielectric pore, and Si nanocrystal diameters.

"Low voltage, scalable nanocrystal FLASH memory fabricated by templated self assembly", K.W. Guarini et al., 2003 IEDM Technical Digest, Session 22.2.

Self Assembled Nanocrystal

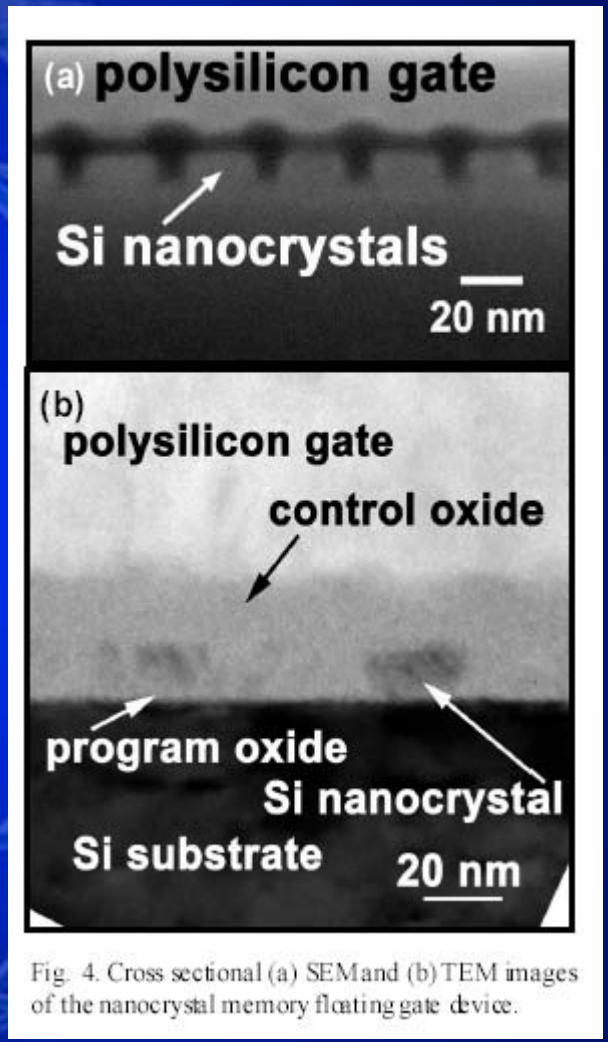


Fig. 4. Cross sectional (a) SEMand (b) TEM images of the nanocrystal memory floating gate device.

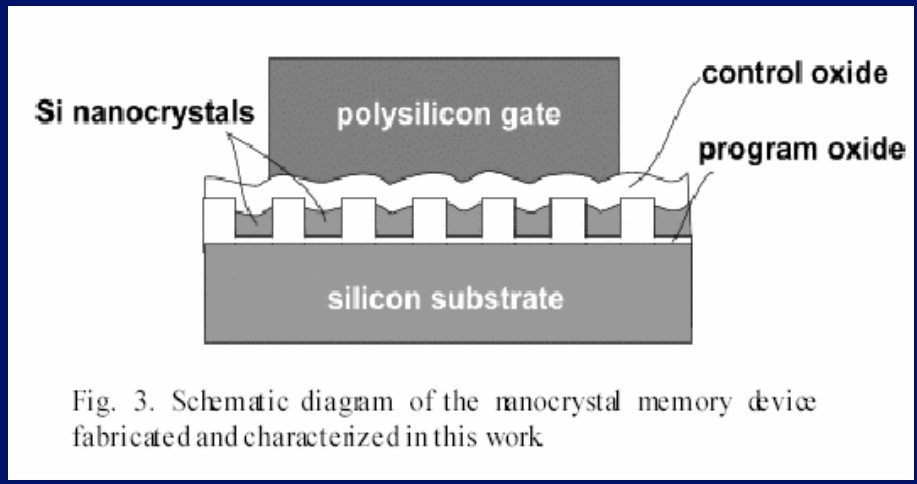


Fig. 3. Schematic diagram of the nanocrystal memory device fabricated and characterized in this work.

- An alternative method for good process control of silicon nanocrystals

"Low voltage, scalable nanocrystal FLASH memory fabricated by templated self assembly", K.W. Guarini et al., 2003 IEDM Technical Digest, Session 22.2.

Barrier Height Modification for Performance Improvement

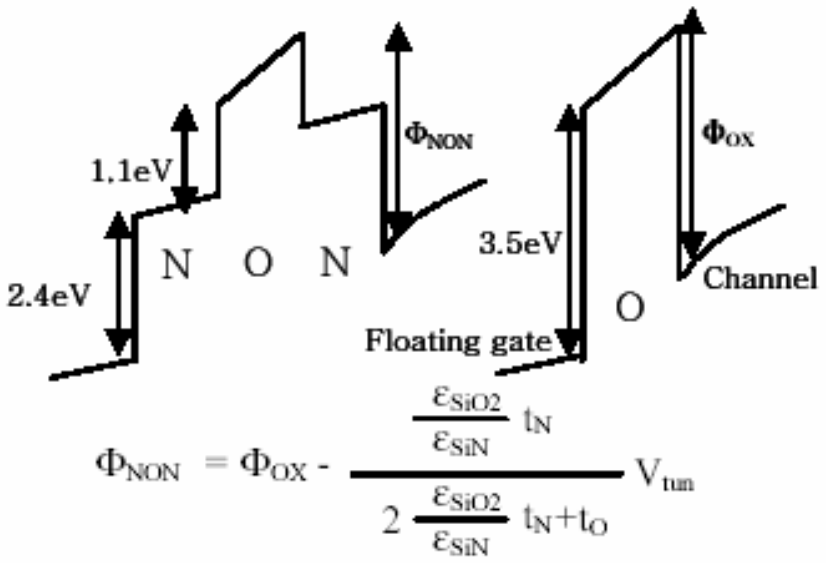


Fig. 6. Barrier height modification of NON stacked tunnel barrier with applied bias. V_{tun} is applied bias across the tunnel barrier. t_N and t_O is the thickness of SiN, SiO_2 layer, respectively

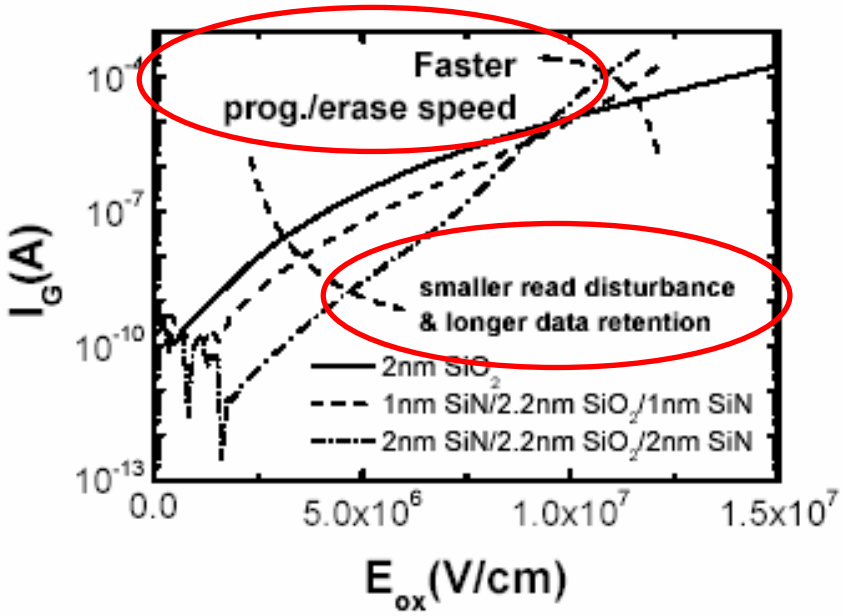


Fig. 7. Tunneling current (I_G) vs. field across the barrier (E_{ox}) for various tunnel barrier structures. The structure of n+ Si/Tunnel barrier/n+ Si is examined.

"High Speed and Nonvolatile Si Nanocrystal Memory for Scaled Flash Technology using Highly Field-Sensitive Tunnel Barrier", S.J. Baik et al., 2003 IEDM Technical Digest, Session 22.3.

Metal Nano Dots

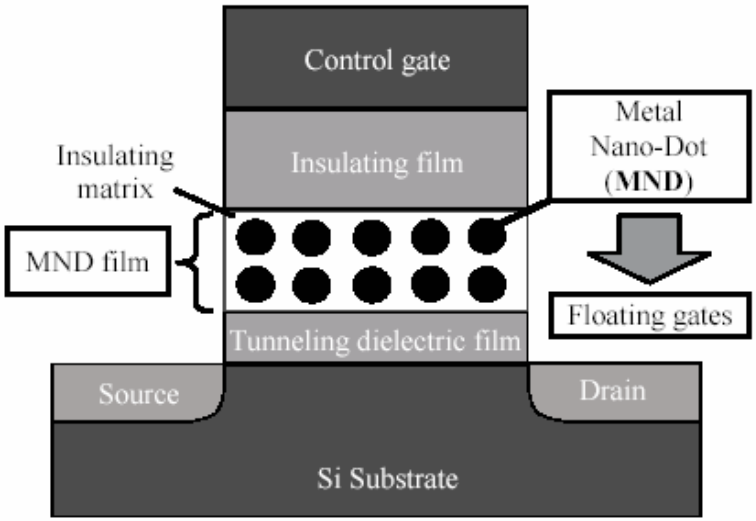


Fig.1 Cross sectional structure of an MND memory cell.

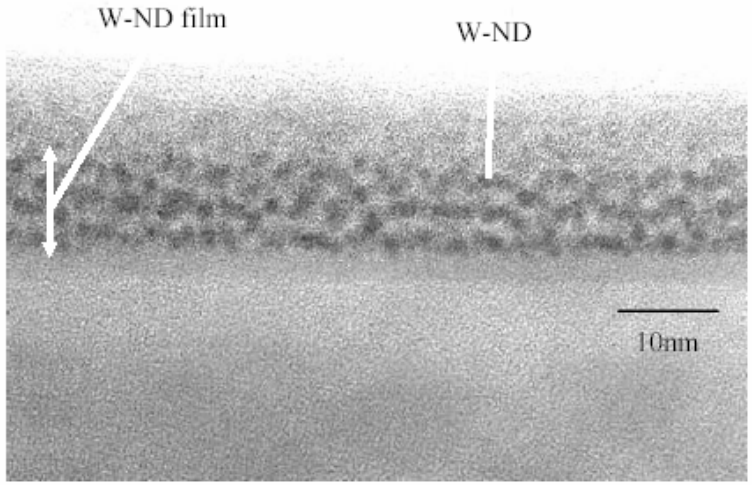


Fig.4 Cross sectional TEM image of W-ND film on a non-alkali glass substrate.

- Instead of silicon islands, metal nano dots can be used for charge storage.

"New Non-Volatile Memory with Extremely High Density Metal Nano-Dots", M. Takata et al., 2003 IEDM Technical Digest, Session 22.5.

Double Layer Metal Dots

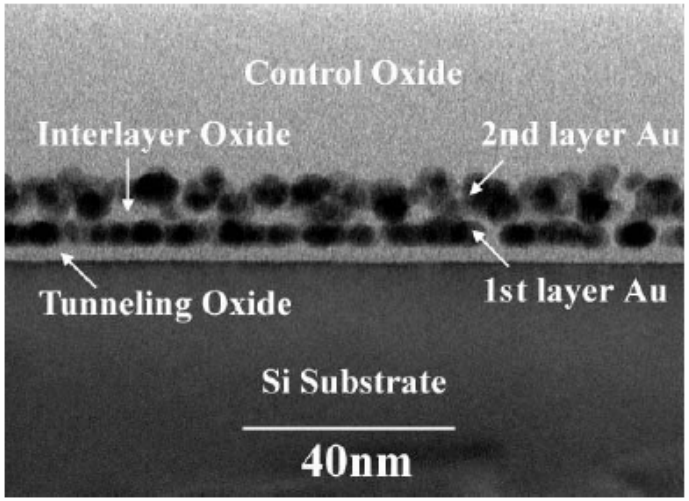


Fig. 15. Bright field STEM cross sectional image. Spherical nanocrystals look overlapped because of the thick sample under STEM.

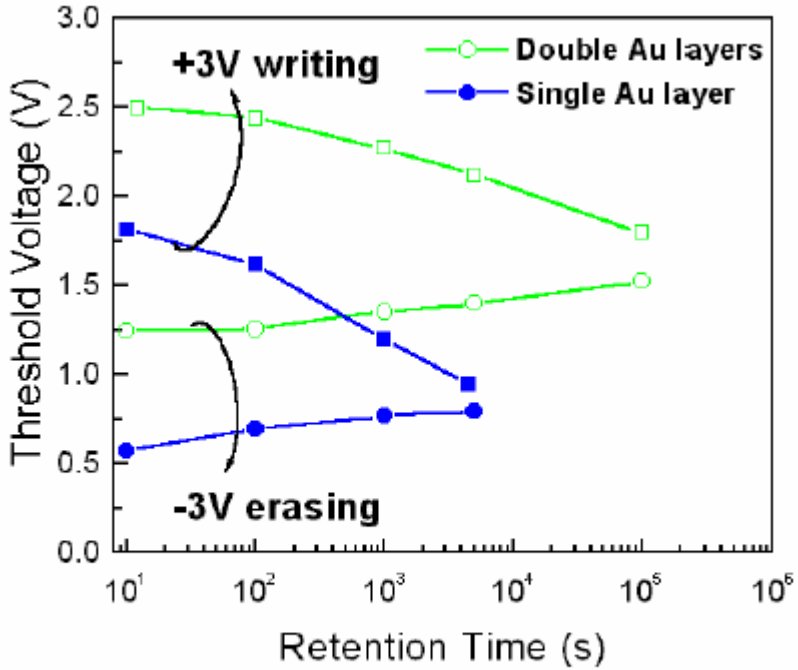


Fig. 16. Retention characteristics of Au double and single layer nanocrystal EEPROM.

- Second Layer metal improves retention

"Operational and Reliability Comparison of Discrete-Storage Nonvolatile Memories: Advantages of Single- and Double- Layer Metal Nanocrystals", C. Lee et al., 2003 IEDM Technical Digest, Session 22.6.

Compact Cell Structure

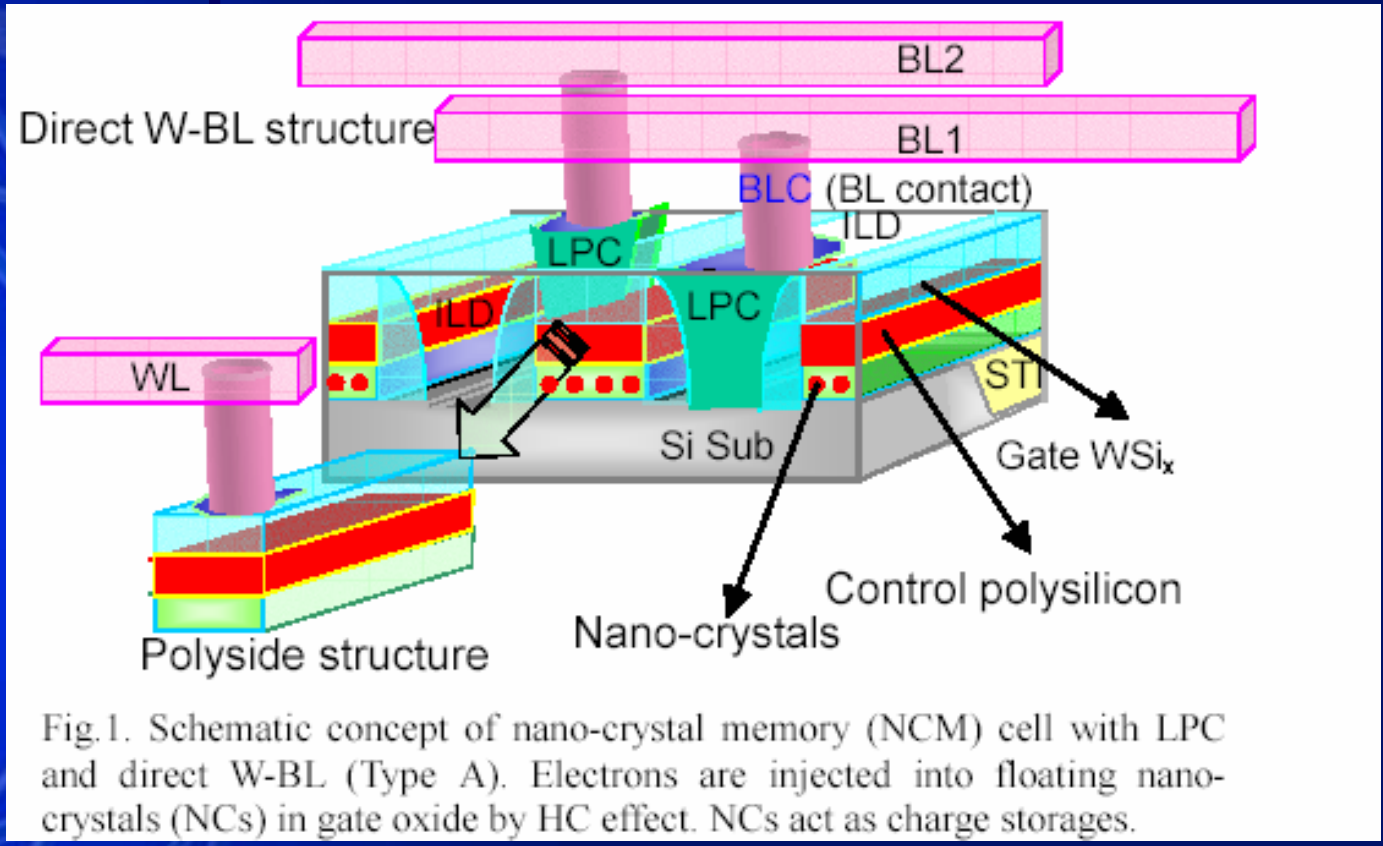


Fig.1. Schematic concept of nano-crystal memory (NCM) cell with LPC and direct W-BL (Type A). Electrons are injected into floating nano-crystals (NCs) in gate oxide by HC effect. NCs act as charge storages.

- With Nanocrystal charge storage, very compact cell can be designed

"Integration of Fluorinated Nano-Crystal Memory Cells with 4.6 F2 Size by Landing Plug Polysilicon Contact and Direct-Tungsten Bitline", I. Kim et al., 2003 IEDM Technical Digest, Session 26.3.

FeFET

Two FeRAM Structures

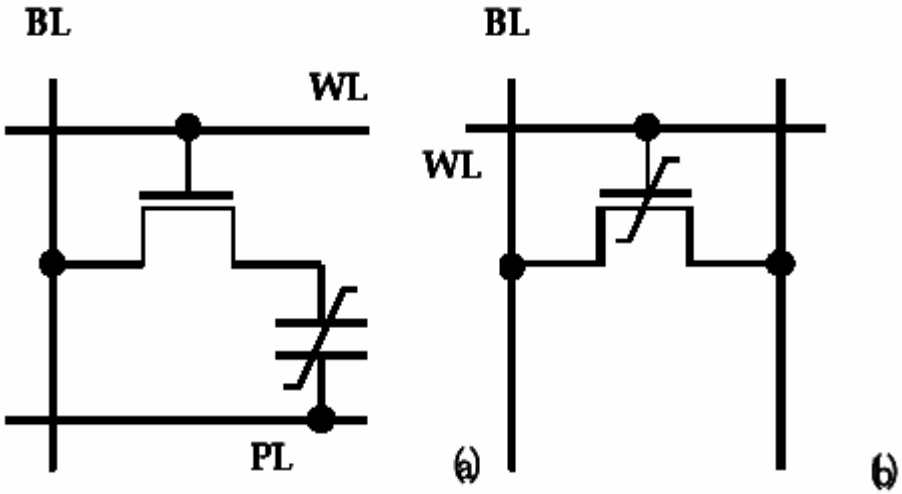


Fig.1 Equivalent circuits of capacitor-type FeRAM (a) and FET-type FeRAM (b).

"Recent Progress in FET-type Ferroelectric Memories", H. Ishiwara, 2003 IEDM Technical Digest, Session 10.5.

- For smaller cell, instead of 1T1C, fold ferro capacitor into gate dielectric
- Challenge is dielectric to silicon interface
  - Buffer layer required -> series capacitance

High K Dielectric for Buffer

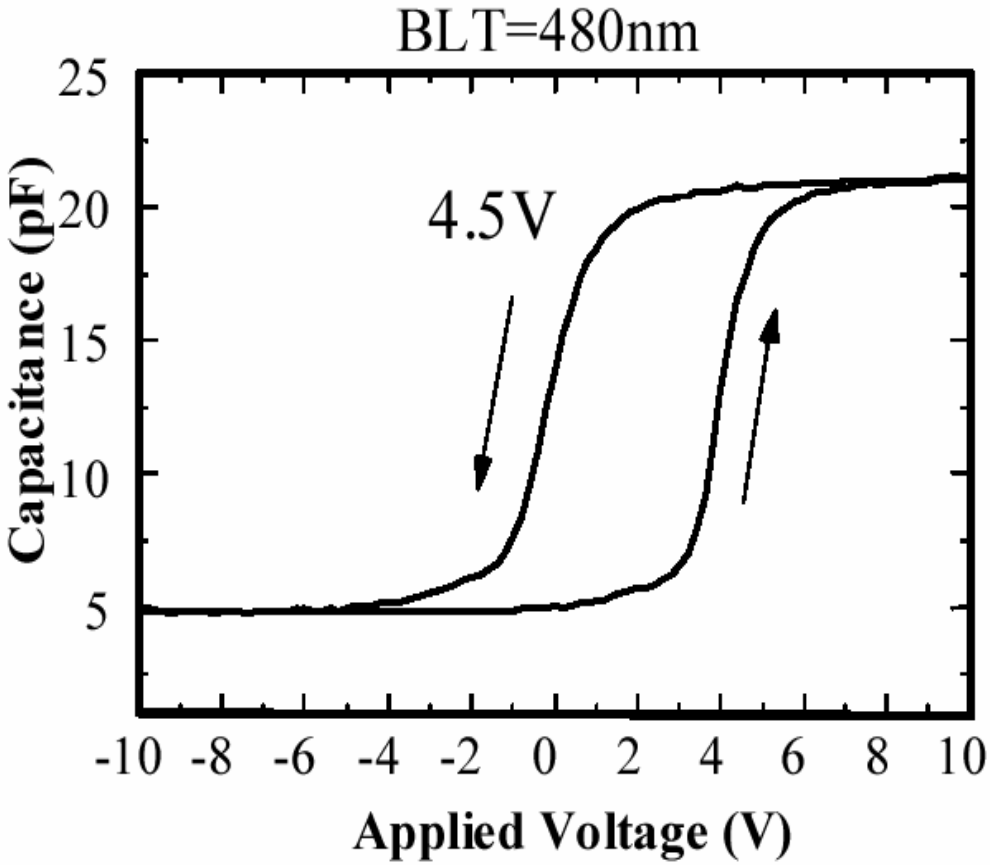


Fig.4 C-V characteristic for a Pt/$(Bi,La)_4Ti_3O_{12}$/$LaAlO_3$/Si diode.

- By using Hi-K dielectric ($LaAlO_3$), series capacitance issue is reduced
- New stack showed good memory window

"Recent Progress in FET-type Ferroelectric Memories", H. Ishiwara, 2003 IEDM Technical Digest, Session 10.5.

Good Storage Characteristics

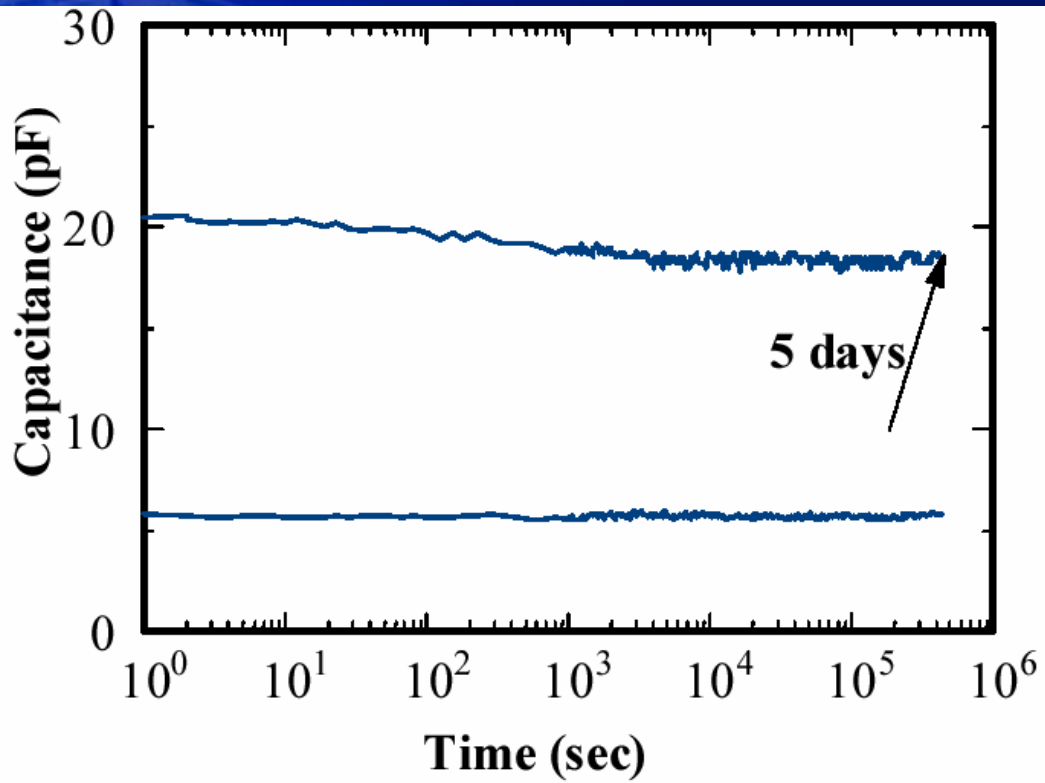


Fig.5 Time dependences of the high and low capacitance values in the Pt/$(Ba,La)_4Ti_3O_{12}$/$LaAlO_3$/Si diode shown in Fig.4.

- With the improved stack, good storage characteristics were observed
- However, still depolarization field -> not a true NVM

"Recent Progress in FET-type Ferroelectric Memories", H. Ishiwara, 2003 IEDM Technical Digest, Session 10.5.

How to Improve FeFET

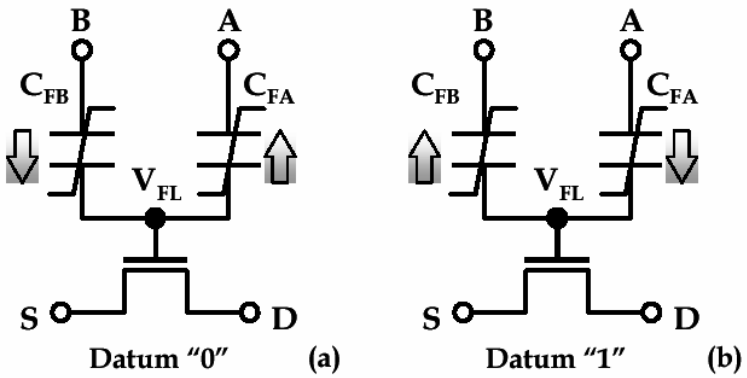


Fig.6 An equivalent circuit of a 1T2C-type ferroelectric memory and the polarization directions for Datum "0" (a) and Datum "1" (b).

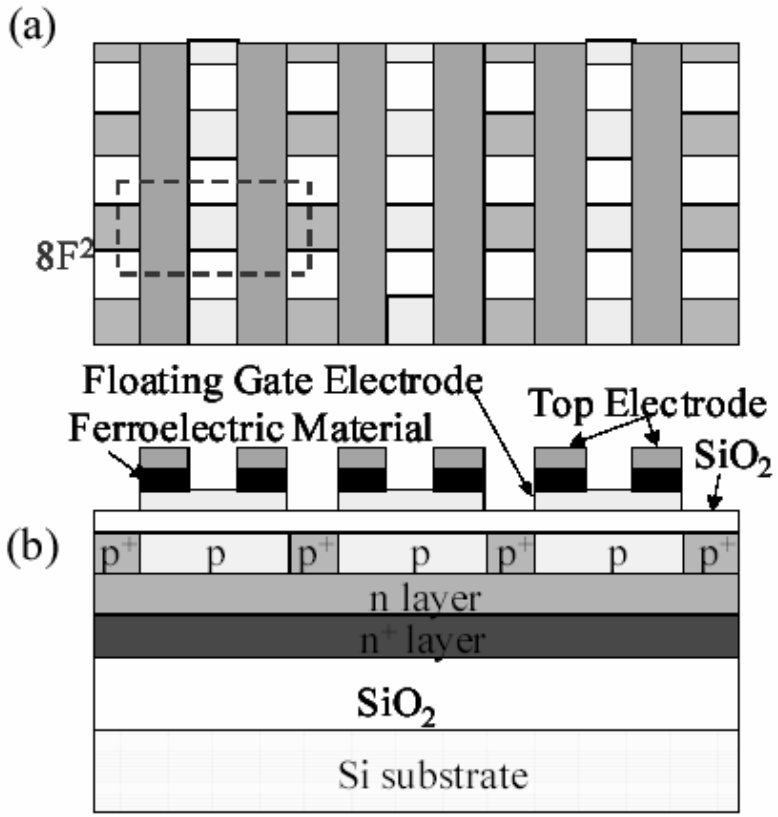


Fig.9 Proposed planar $8F^2$ cell array. (a) top view and (b) cross section along a Si stripe.

"Recent Progress in FET-type Ferroelectric Memories", H. Ishiwara, 2003 IEDM Technical Digest, Session 10.5.

Retention Improvement

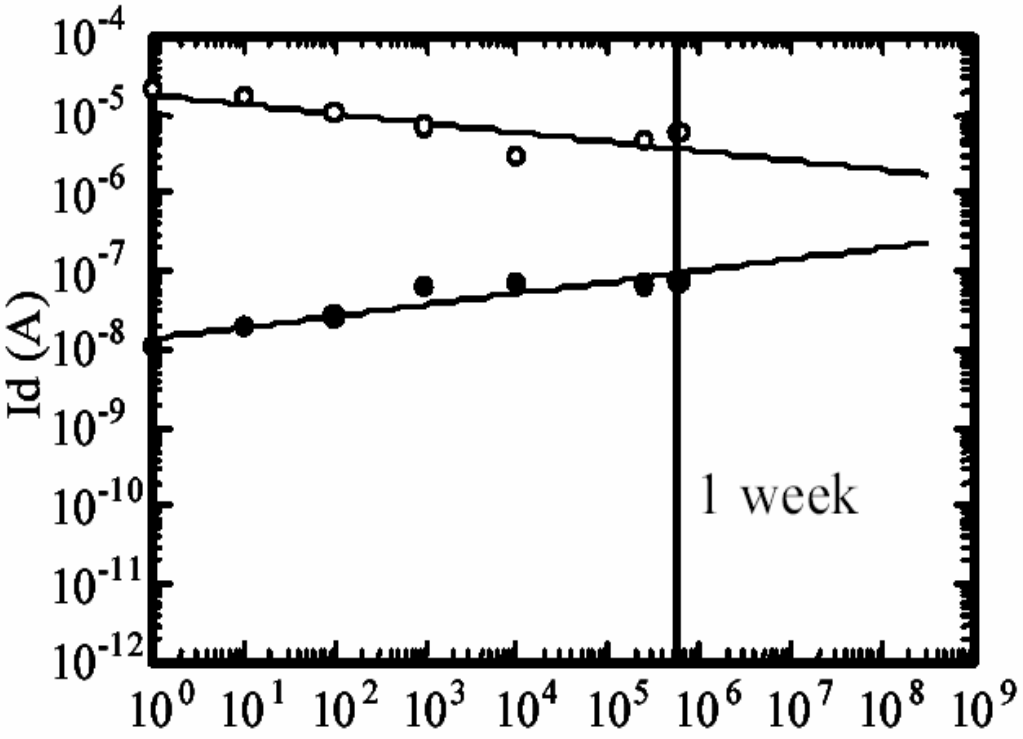


Fig.8 Data retention characteristics in a 1T2C-type cell. The edge of the extrapolated lines corresponds to 10 years.

- By using two capacitors written in opposite polarization, long storage time achieved
- Cell Size is larger

"Recent Progress in FET-type Ferroelectric Memories", H. Ishiwara, 2003 IEDM Technical Digest, Session 10.5.

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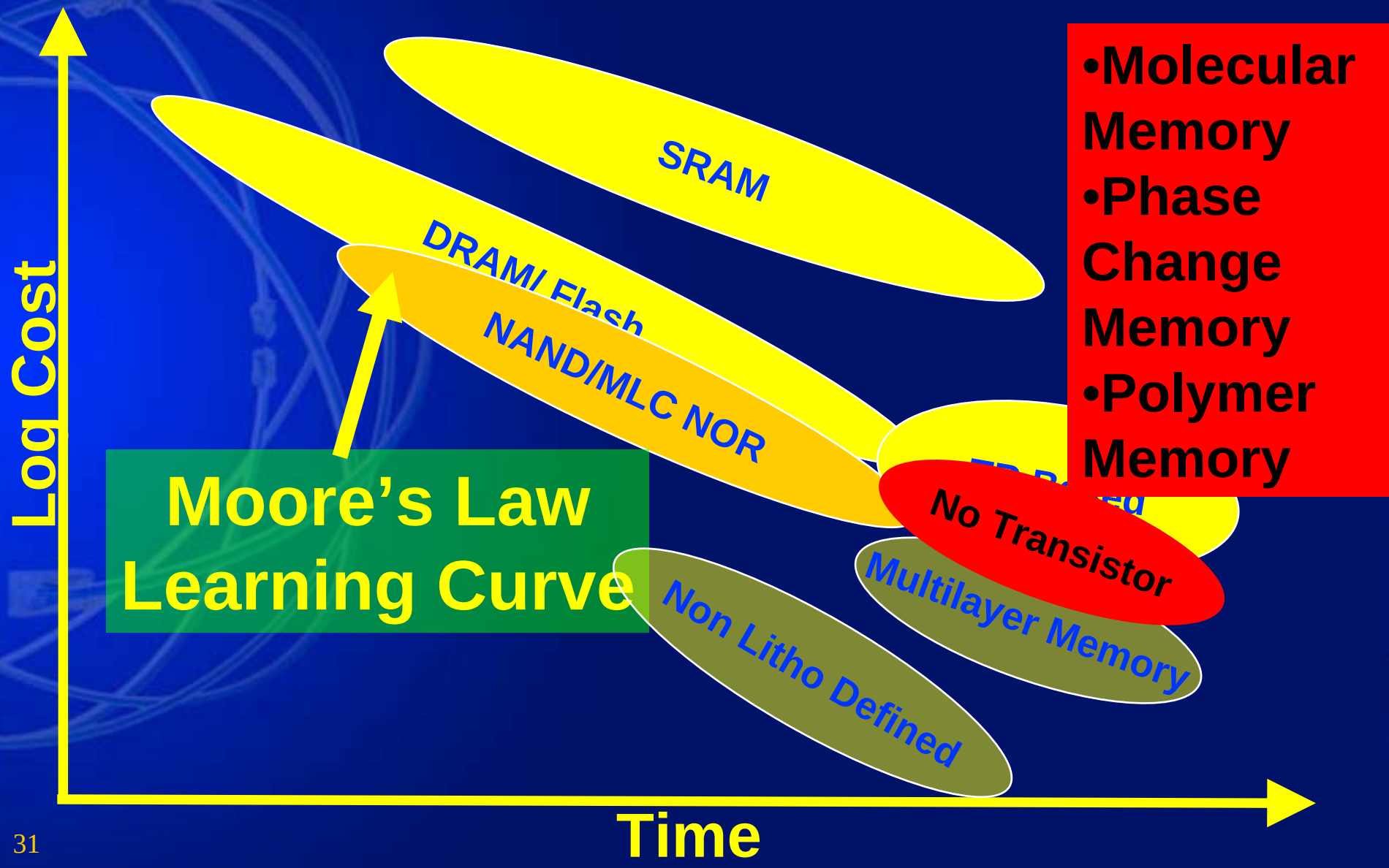
Memory Cost Projection



- Molecular Memory
- Phase Change Memory
- Polymer Memory

Molecular Memory

Molecular Memory

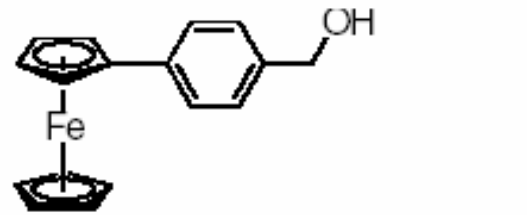


Figure 1b. Molecular structure of Fc-BzOH.

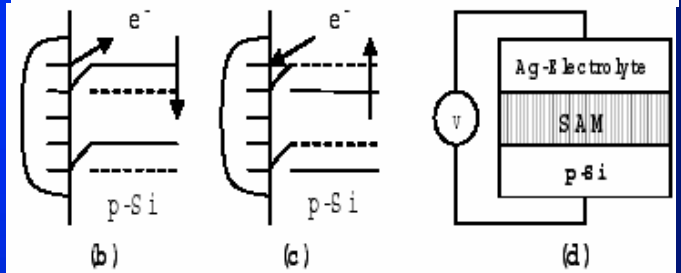


Figure 3 (b) and (c) Energy band diagrams for oxidation and reduction of the molecules respectively. The former corresponds to the read cycle while the latter corresponds to the write cycle. (d) Schematic equivalent of the electrical connections for characterization.

"Hybrid Silicon/Molecular Memories: Co-Engineering for Novel Functionality", S. Gowda et al., 2003 IEDM Technical Digest, Session 22.1.

- Molecules showed Redox charge transport properties that can be used for memory storage
- Properly designed molecules can have multi-level storage

Information Storage

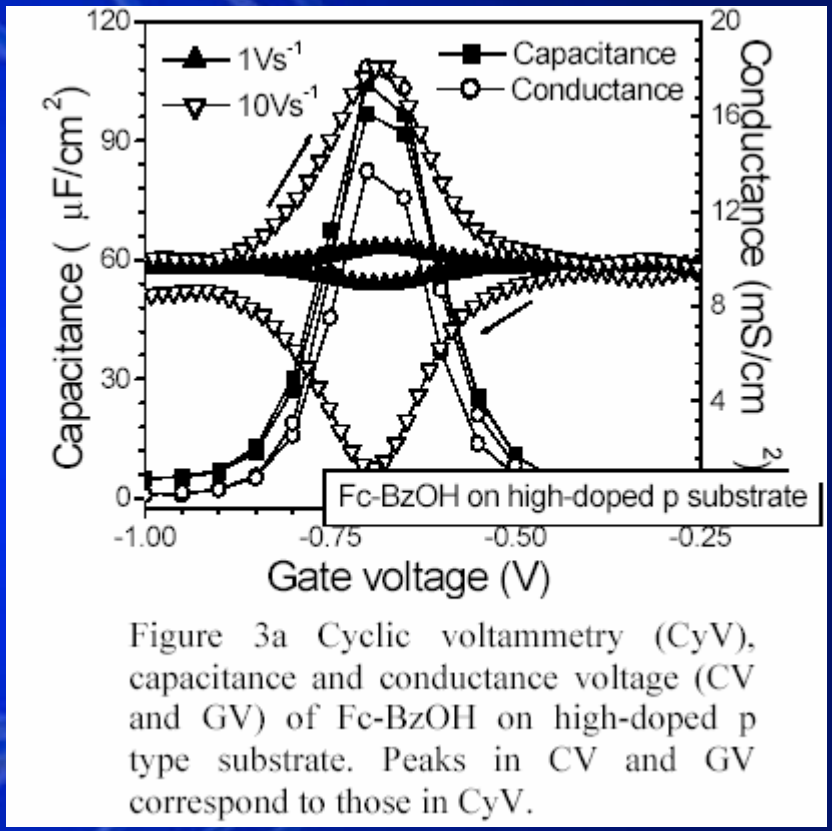


Figure 3a Cyclic voltammetry (CyV), capacitance and conductance voltage (CV and GV) of Fc-BzOH on high-doped p type substrate. Peaks in CV and GV correspond to those in CyV.

"Hybrid Silicon/Molecular Memories: Co-Engineering for Novel Functionality", S. Gowda et al., 2003 IEDM Technical Digest, Session 22.1.

- Bias applied by ramping voltage drive electrons in and out giving a capacitance/ conductance peak, which is sensed
- Read is destructive in 1C1T memory

Phase Change Memory

Cell current reduction: Reduce contact size

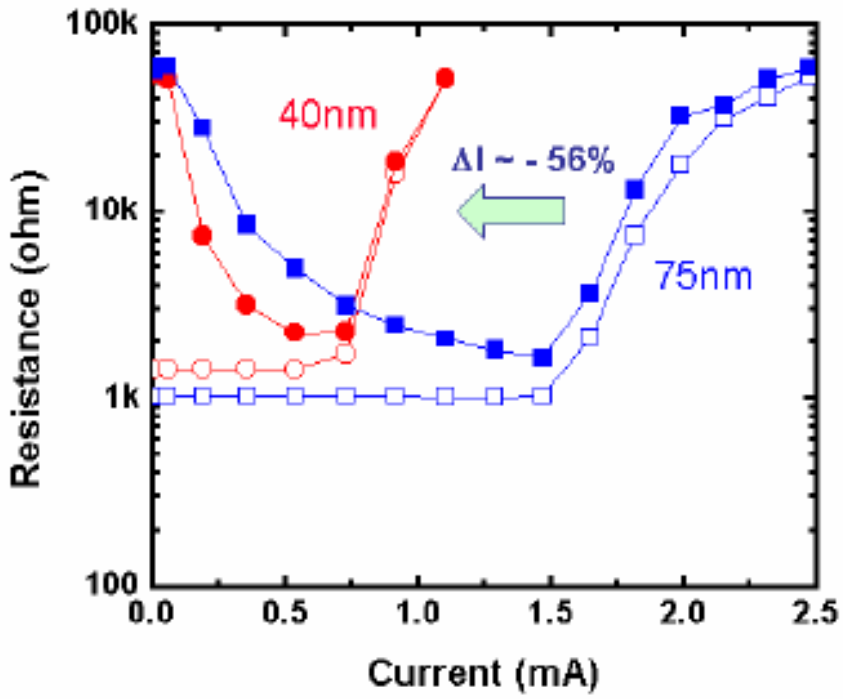


Figure 6. The R-I curves measured in two cell elements having different BEC contact size. As BEC size reduces from 75nm to 40nm, the writing current decreases drastically from 2.0mA to 0.9mA.

- The focus effort in phase change memory is in program current reduction

"Writing Current Reduction for High-density Phase-change RAM", Y. Hwang et al., 2003 IEDM Technical Digest, Session 37.1.

Confined GST Structure

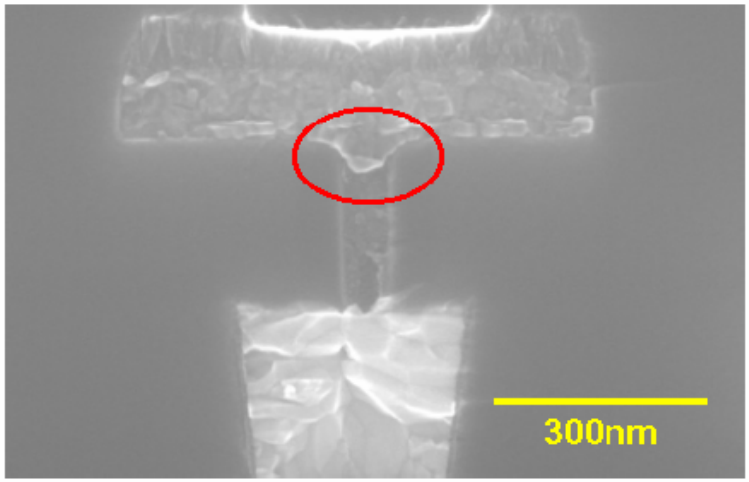


Figure 12. The confined GST structure. After BEC is filled with CVD TiN and is polished by CMP process, the filled TiN is slightly removed and then GST is deposited to localize current distribution.

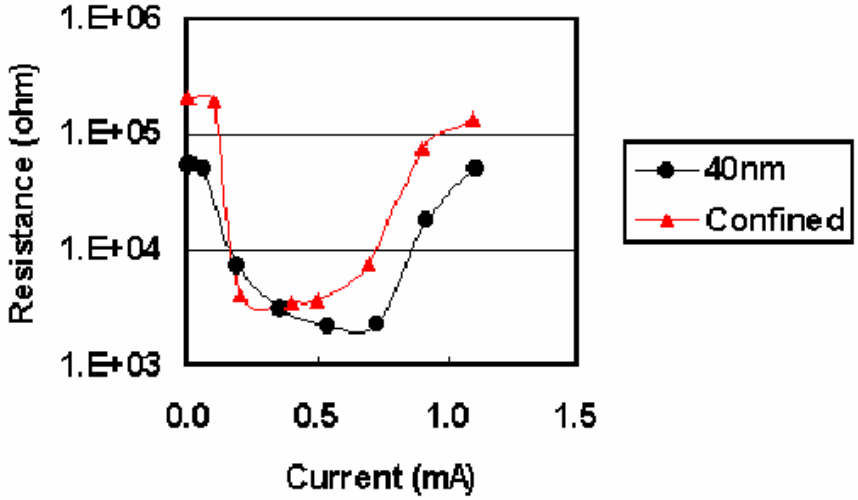


Figure 13. The R-I curve of the confined GST structure shows that the writing current can be reduced by a slight modification of cell structure for localization of current

- Current is further reduced by controlling the thermal environment

"Writing Current Reduction for High-density Phase-change RAM", Y. Hwang et al., 2003 IEDM Technical Digest, Session 37.1.

Other methods for Current Reduction

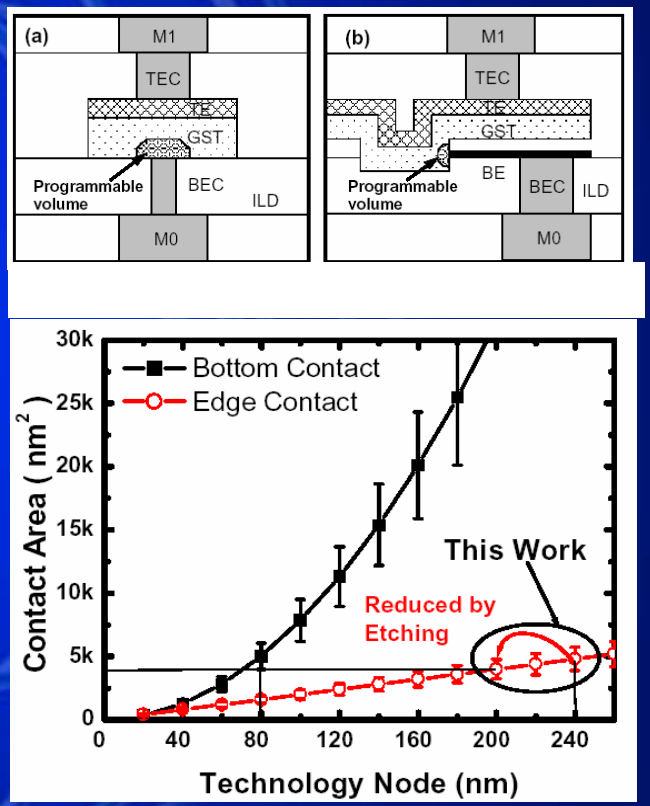
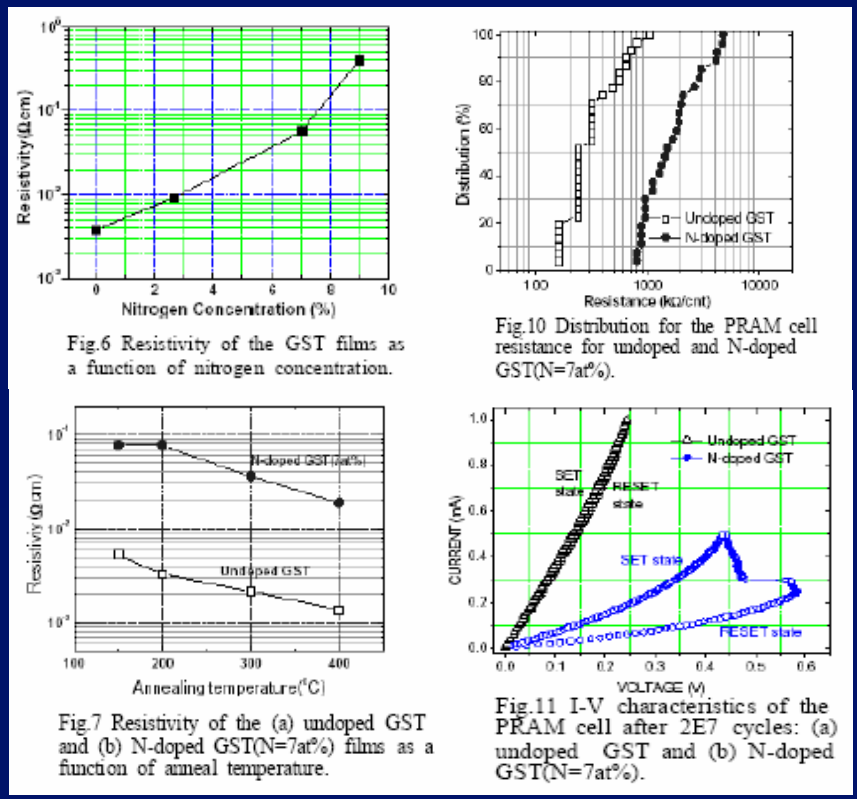


Figure 8: Edge contact current reduction

- Edge contact



- Nitrogen Doping

W Heater and ON-Plug

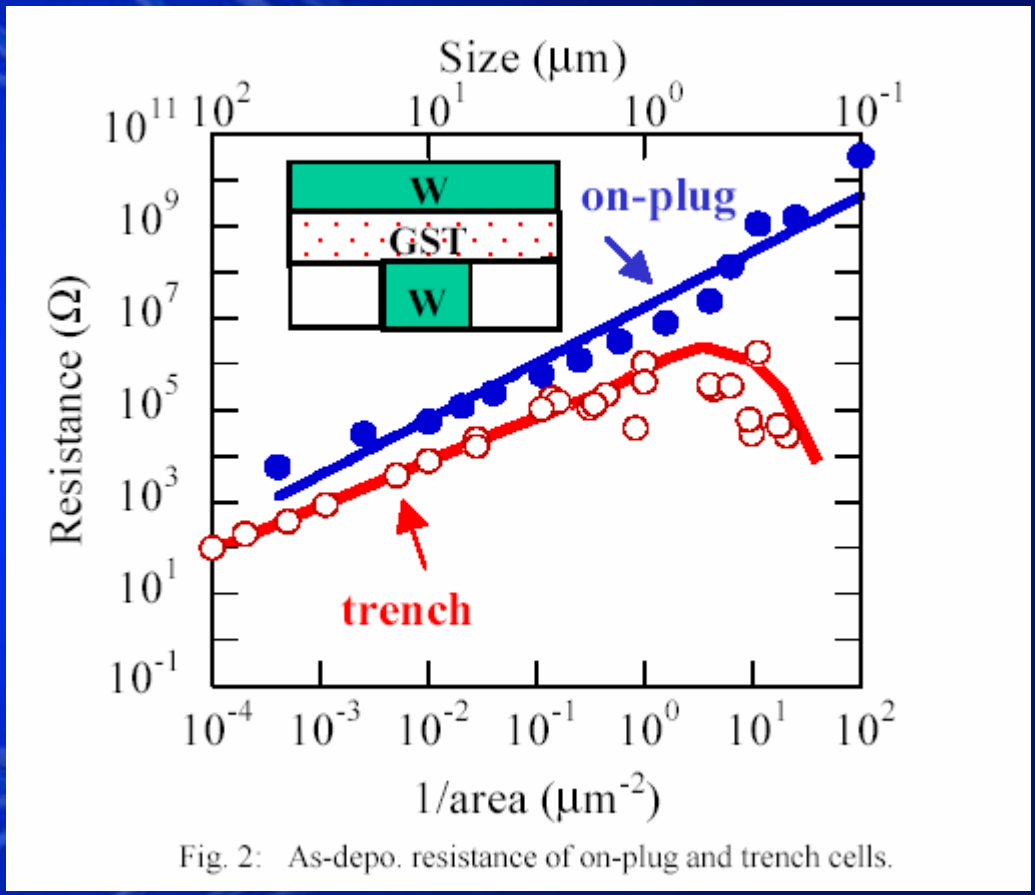


Fig. 2: As-depo. resistance of on-plug and trench cells.

- Using W as contact material and a confined geometry, low program current is observed

"A GeSbTe Phase-Change Memory Cell Featuring a Tungsten Heater Electrode for Low-Power, Highly Stable, and Short-Read-Cycle Operations", N. Takaura et al., 2003 IEDM Technical Digest, Session 37.2.

Tungsten Heater

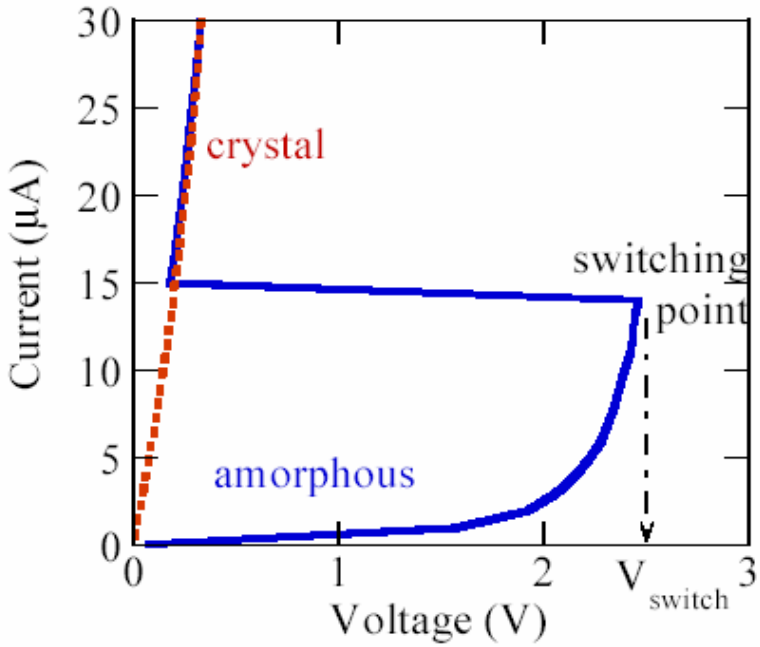


Fig. 3: *I-V* curves of a (0.16 μm)² on-plug cell. Values for amorphous material are for the as-depo. state.

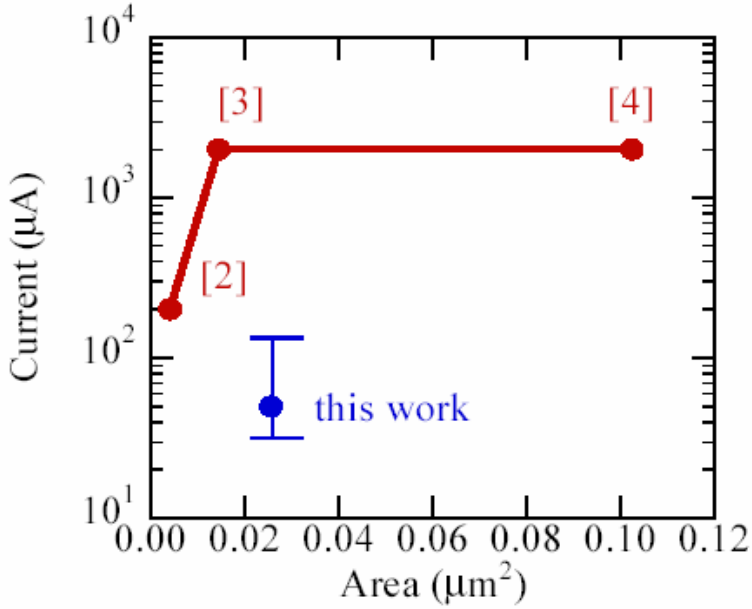


Fig. 10: Comparison of reset current. The current of 50 μA in this work is the lowest ever reported.

"A GeSbTe Phase-Change Memory Cell Featuring a Tungsten Heater Electrode for Low-Power, Highly Stable, and Short-Read-Cycle Operations", N. Takaura et al., 2003 IEDM Technical Digest, Session 37.2.

- The 15 μa switch current with (0.16 μm)² is the lowest reported so far

Metal Layer Inserted

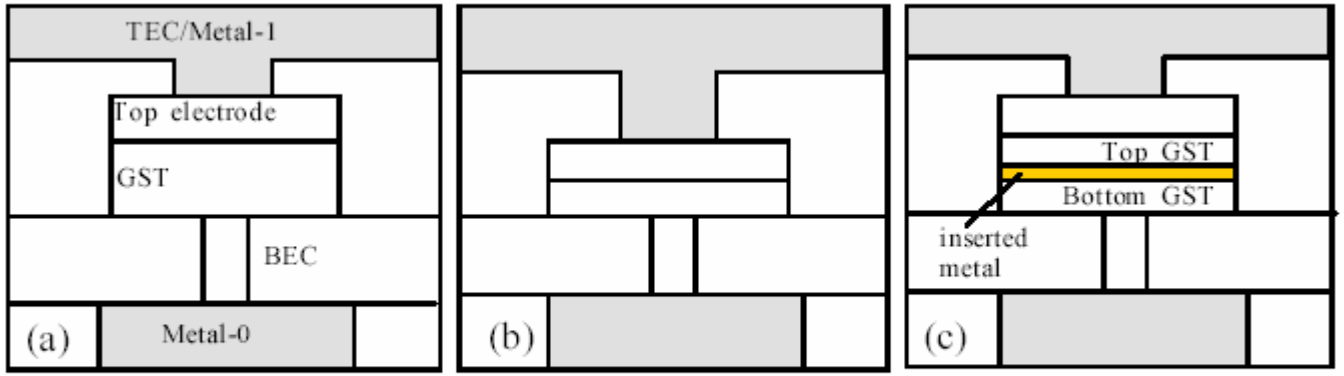


Fig.6 Test structures of (a) single layer of 100nm, (b) single layer of 50nm and (c) novel metal inserted (bottom GST=50nm, inserted TiN~7.5nm, and top GST=50nm thickness each) cell

- Another novel approach: insert metal layers in between two GST layers
- Improves thermal environment and lowers program current

"Novel Cell Structure of PRAM with thin metal layer inserted GeSbTe", J. Yi et al., 2003 IEDM Technical Digest, Session 37.3.

Effect of Multilayer

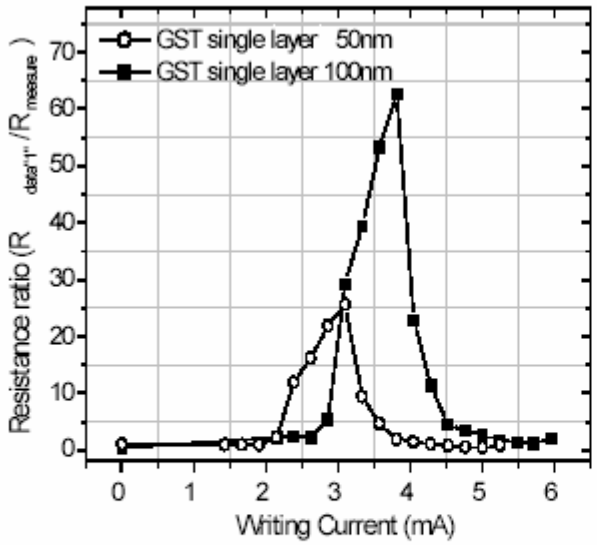


Fig.8 Resistance ratio vs. writing current for the single layered structure, thickness of 50nm and 100nm. Each curve is taken for same pulse width, 30ns

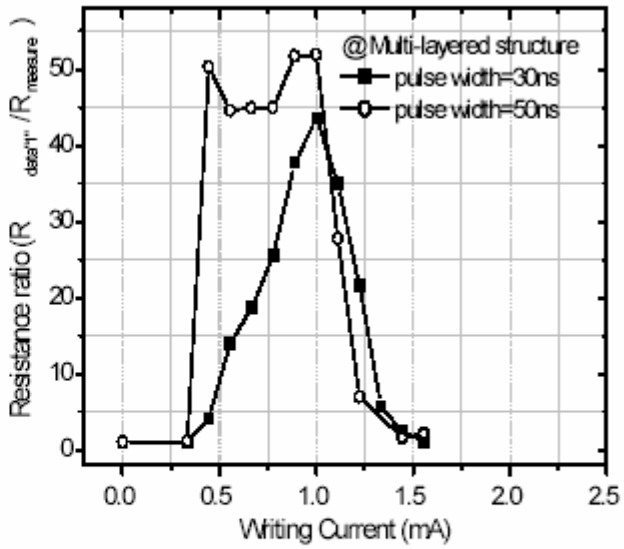


Fig.9 Resistance ratio vs. writing current for the metal inserted cell structure (GST 50nm/TiN 7.5nm/GST 50nm) Curves are drawn for different pulse width.

- Write current is reduced compared to single layer

"Novel Cell Structure of PRAM with thin metal layer inserted GeSbTe", J. Yi et al., 2003 IEDM Technical Digest, Session 37.3.

Zero Transistor Cell

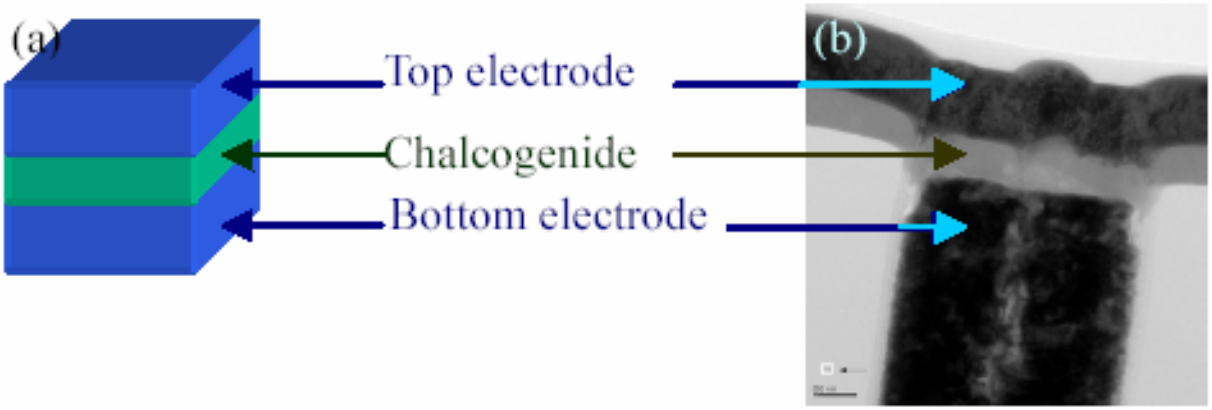


Fig. 1 The structure of a TF-RRAM device. (a) A cell contains top electrode, chalcogenide layer, and bottom electrode. (b) A cross-sectional TEM picture of the device studied in this work. The top electrode, chalcogenide, and bottom electrode are TiW, $Ge_2Sb_2Te_5$, and W, respectively

- For simplest structure and lowest cost, a zero transistor cell is proposed
- It relies on threshold switching properties in the amorphous states

"An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device", Y. Chen et al., 2003 IEDM Technical Digest, Session 37.4.

Zero Transistor Cell

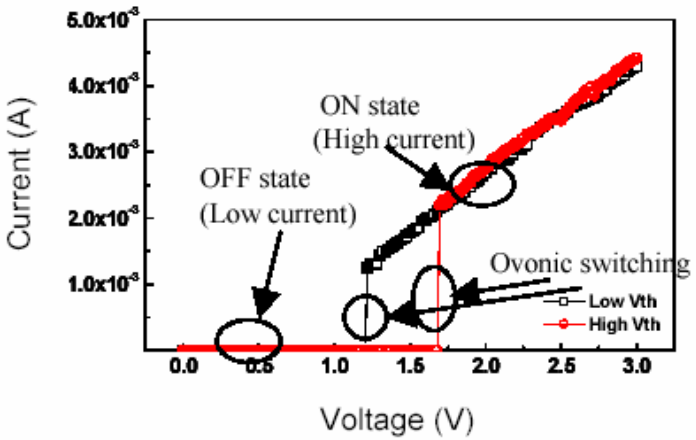


Fig. 2 The I-V curve of a TF-RRAM device. Ovonic switching, "OFF" state, and "ON" state of the device are shown. The open squares represent the I-V curve of a device with Vth=1.2 V and the circles show the I-V curve of a device with Vth=1.7 V.

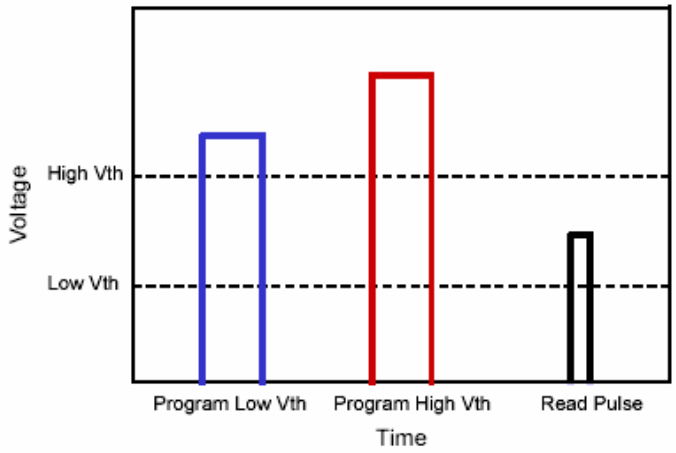
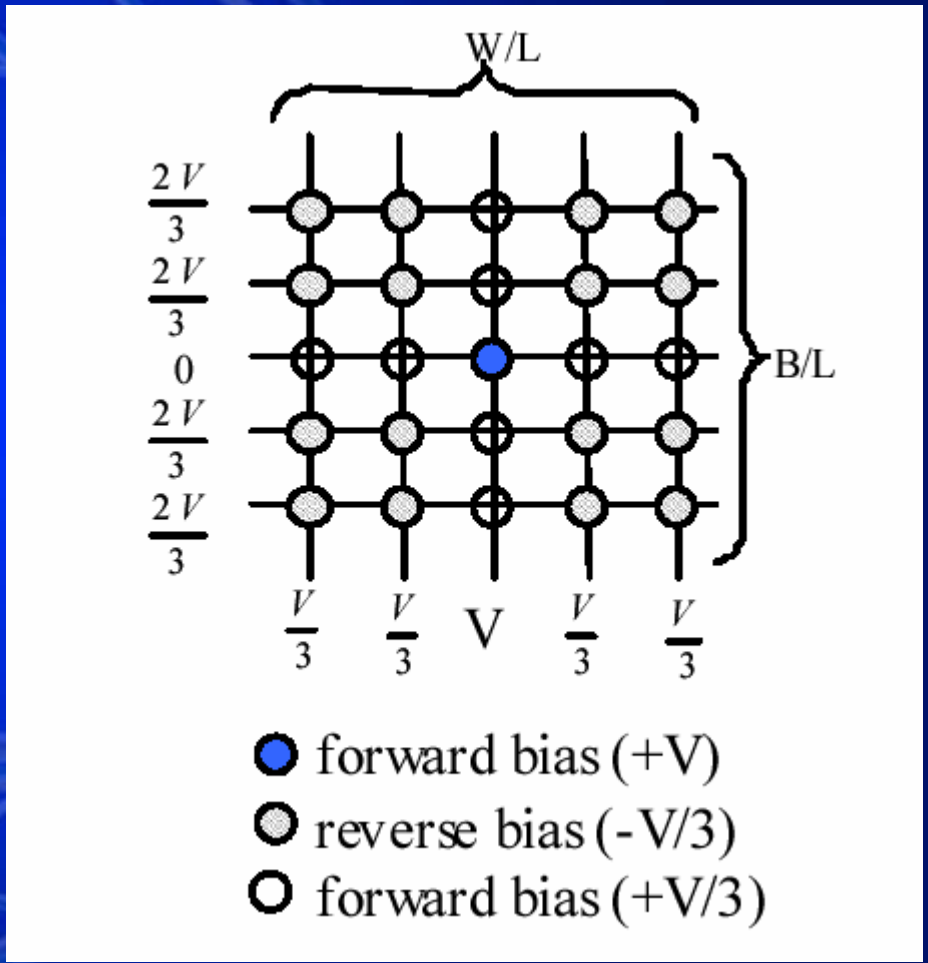


Fig. 3 The pulses for programming low Vth, high Vth, and for reading. Both programming pulses have higher voltages than the high Vth. The read pulse voltage is between the two Vths and the read pulse width is short.

- Cell is never switched to the crystalline state
- Cell is switched between low and high threshold voltages
- Short read pulse between high and low threshold

"An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device", Y. Chen et al., 2003 IEDM Technical Digest, Session 37.4.

Array Inhibit



- Using V/3 in array, disturb is minimized
  - Cross point cell gets full V
  - Other cells get at most positive or negative V/3

"An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device", Y. Chen et al., 2003 IEDM Technical Digest, Session 37.4.

Array Architecture

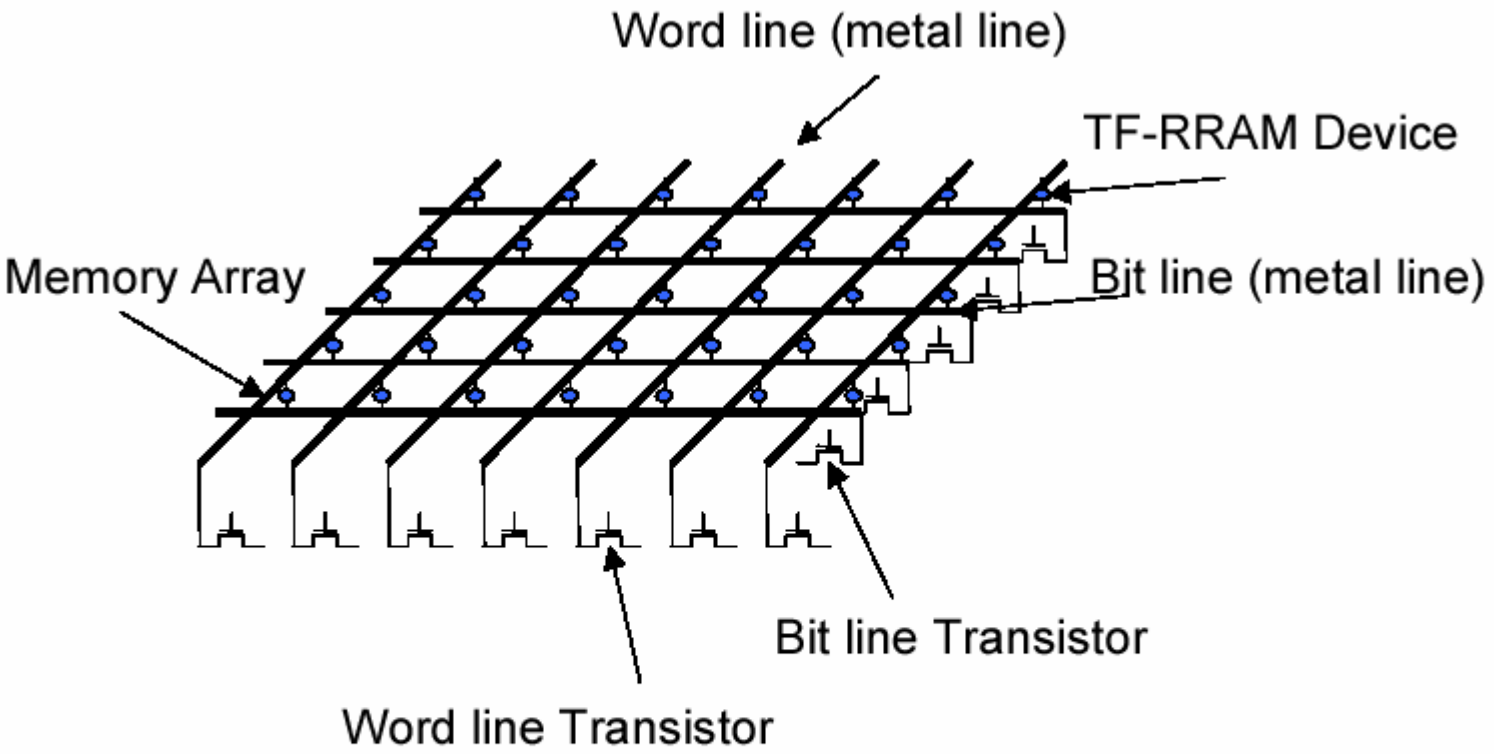


Fig. 4 A schematic of the architecture of TF-RRAM memory array. The word lines and the bit lines are selected by word line transistors and bit line transistors, respectively. The TF-RRAM device serves both as the memory element and as the access element.

"An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device", Y. Chen et al., 2003 IEDM Technical Digest, Session 37.4.

TEM of Array

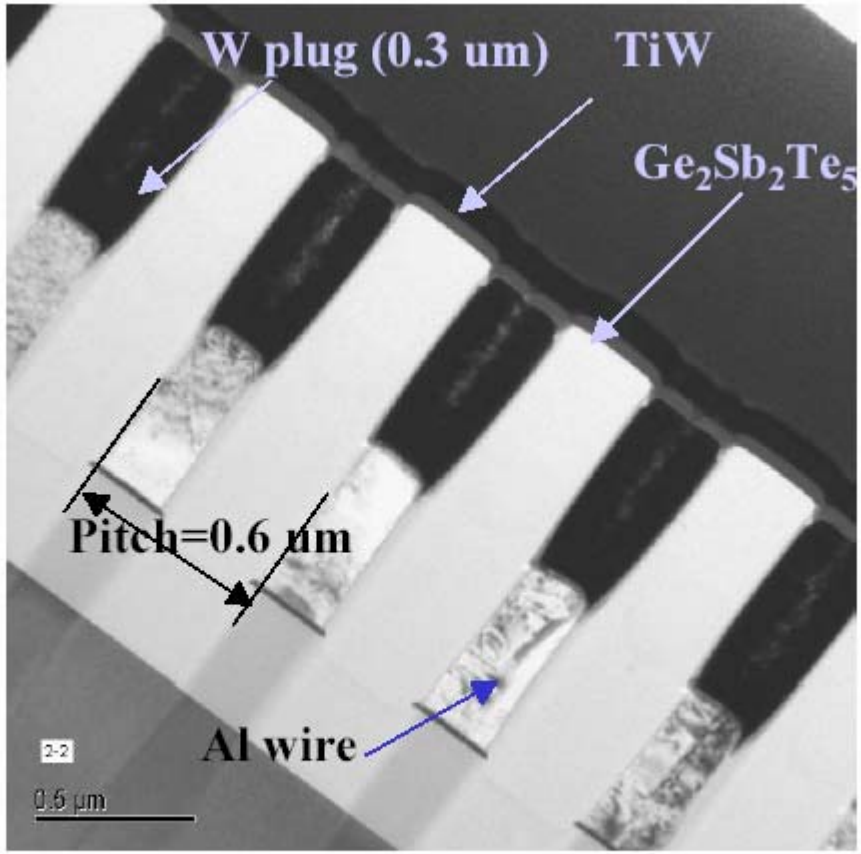
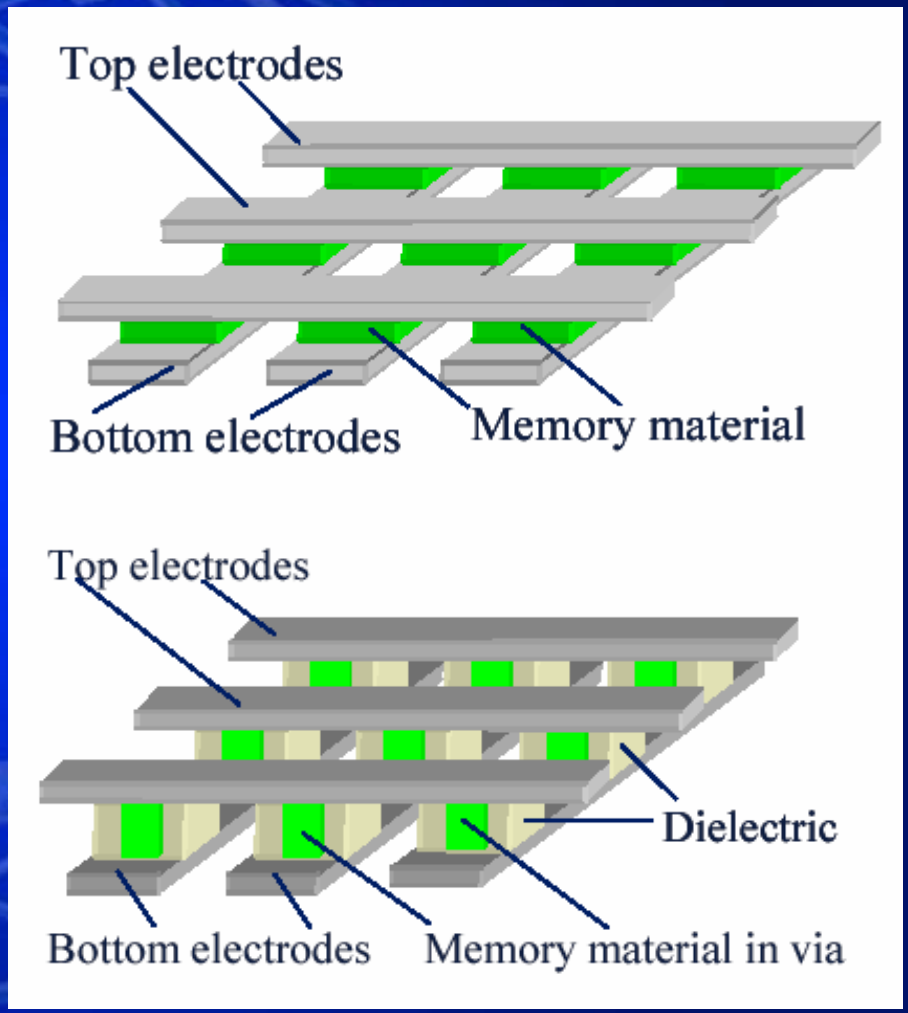


Fig. 12 Bright field TEM picture of the mini array. The diameter plugs is 0.3 µm and the pitch of the mini-array is 0.6 µm.

"An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using a Novel Threshold Switching, Self-Rectifying Chalcogenide Device", Y. Chen et al., 2003 IEDM Technical Digest, Session 37.4.

Polymer Memory

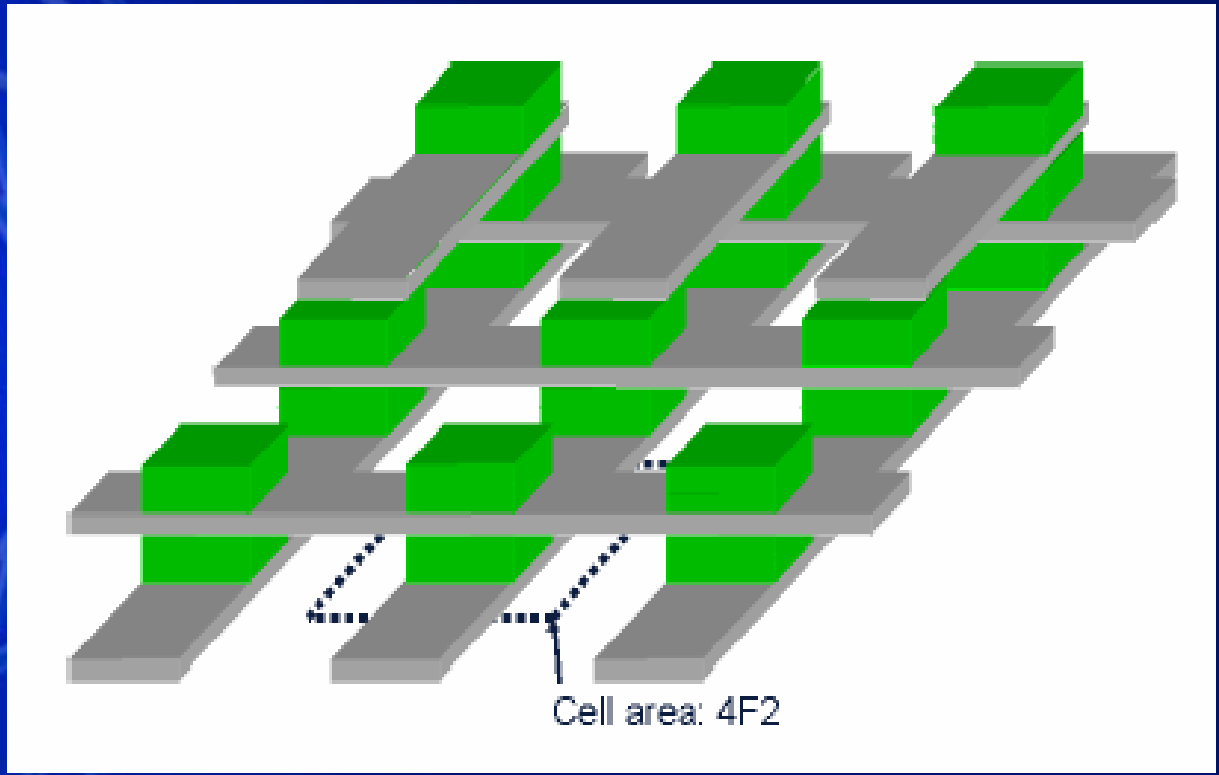
Polymer Memory



- Low cost polymer at cross point of metal layers
  - Resistance change
  - Low cost back end process
  - Better noise with dielectric isolation

"Organic Materials for High-Density Non-Volatile Memory Applications", R. Sezi et al., 2003 IEDM Technical Digest, Session 10.2.

Multilayer for Lower Cost



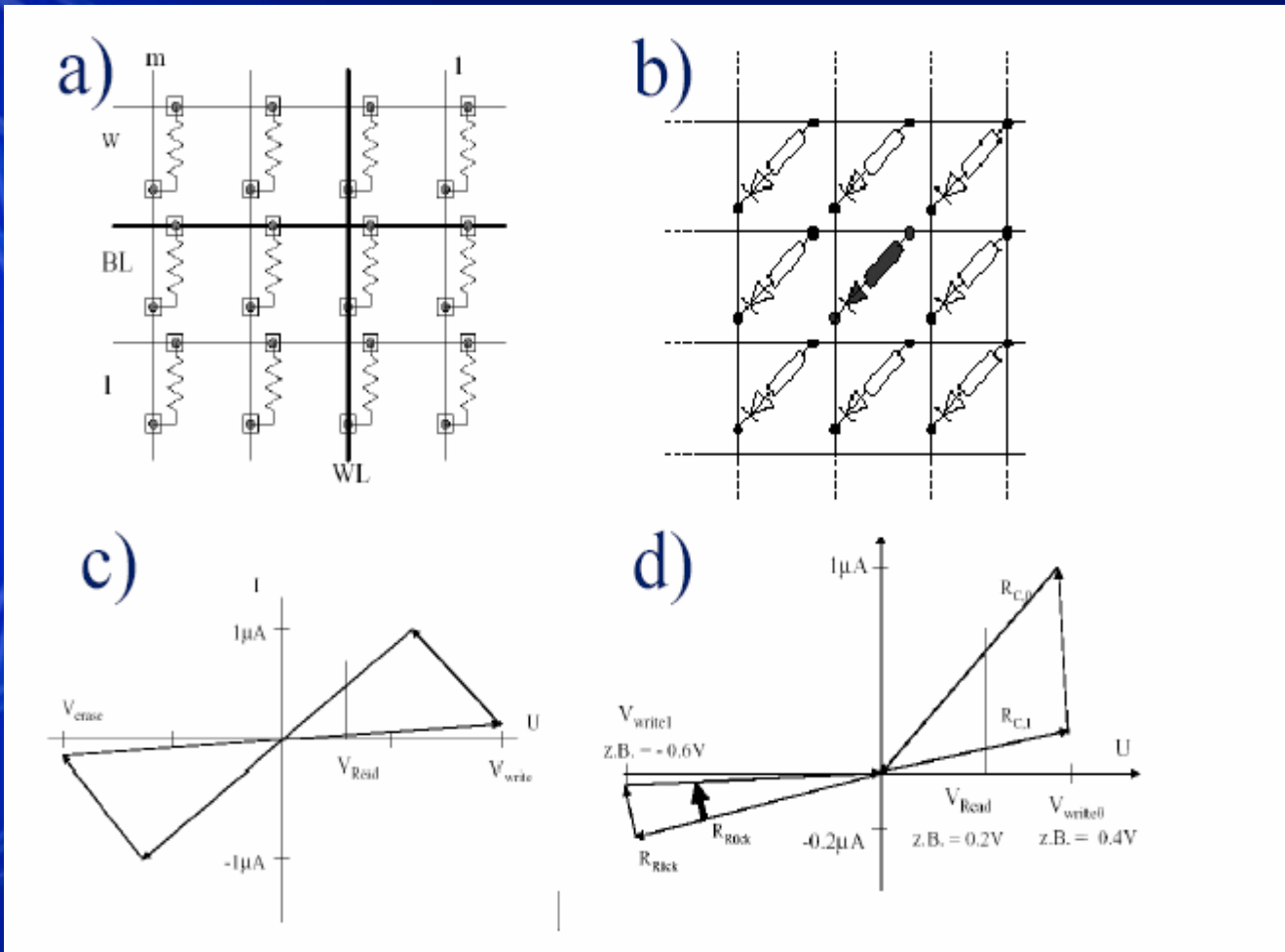
"Organic Materials for High-Density Non-Volatile Memory Applications", R. Sezi et al., 2003 IEDM Technical Digest, Session 10.2.

Technology Parameters

PROPERTY	REQUIREMENT
Switching voltage	$\leq$ 3V
Retention	10 years @85°C
Endurance	$\geq 10^6$ w/e cycles
Read cycles	unlimited
Cell size	4-8F2/n
Scalability	$\leq$ 20x20 nm^2
Temperature stability	$\geq$ 350°C
Electrode material	Standard Al or Cu metallization

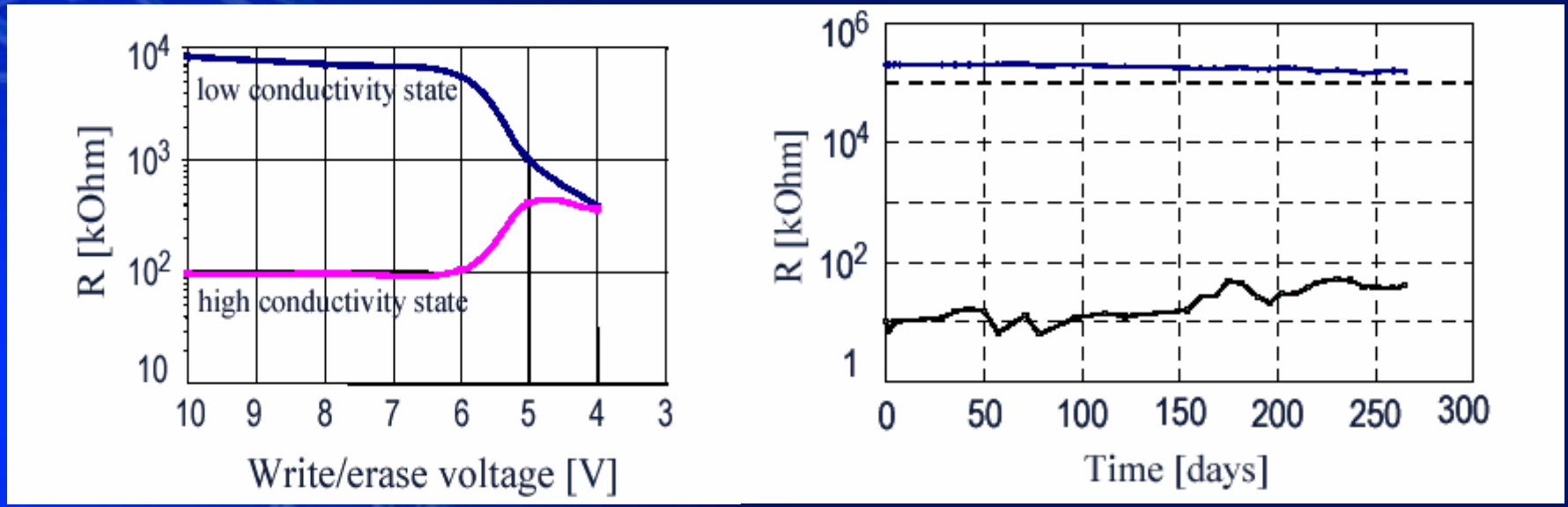
"Organic Materials for High-Density Non-Volatile Memory Applications", R. Sezi et al., 2003 IEDM Technical Digest, Session 10.2.

Array Architecture and IV



"Organic Materials for High-Density Non-Volatile Memory Applications", R. Sezi et al., 2003 IEDM Technical Digest, Session 10.2.

Cell Performance



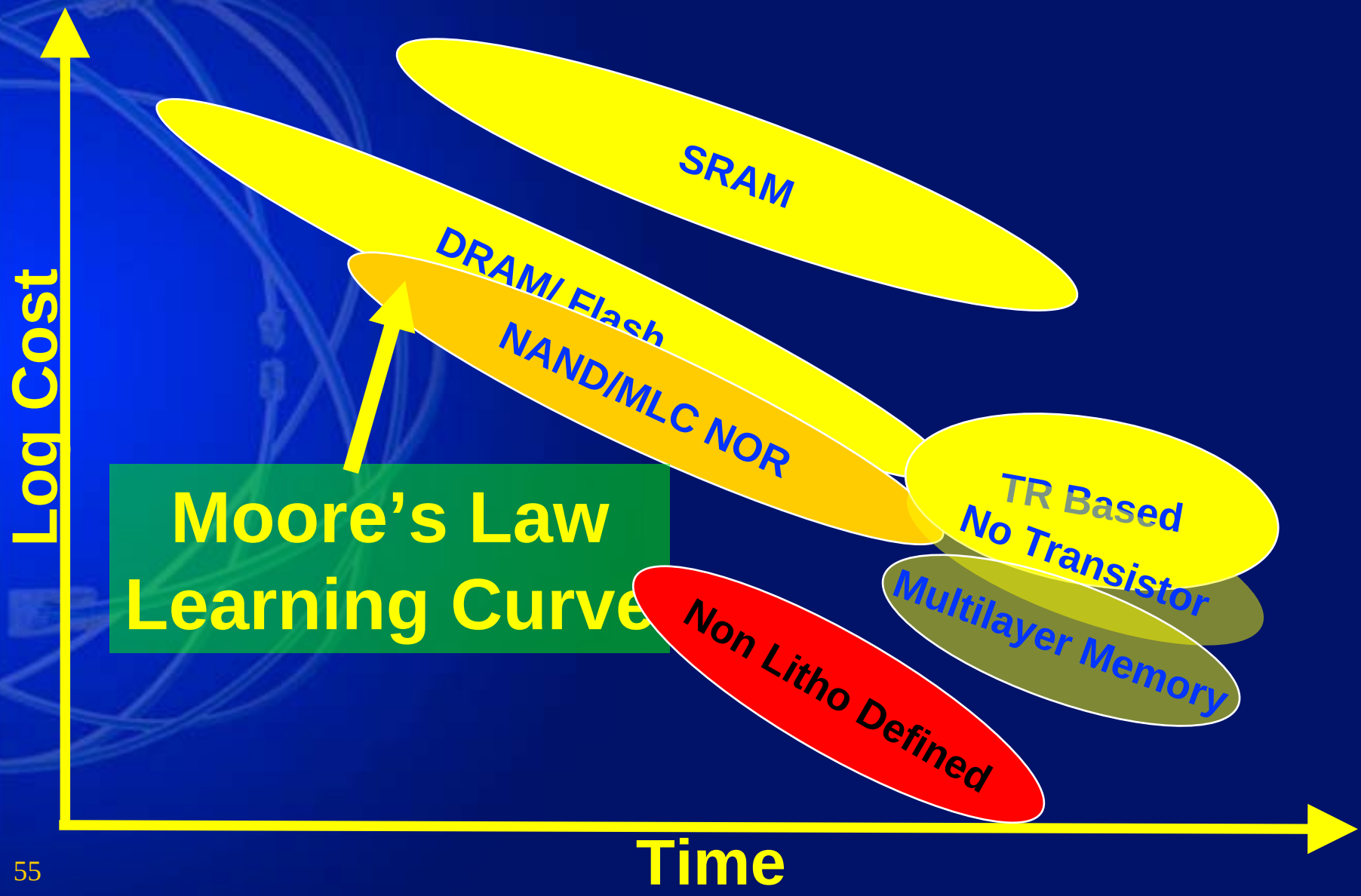
- Good window observed for >6V
- Retention time of many months reported

"Organic Materials for High-Density Non-Volatile Memory Applications", R. Sezi et al., 2003 IEDM Technical Digest, Session 10.2.

Agenda

- Introduction
- Transistor Based Memory Scaling
- No Transistor Memories
- Non Litho Defined Memories
- Summary

Memory Cost Projection



Millipede Memory

Millipede Memory

- Operation
  - Basic concept similar to punch cards
  - Thermally assisted, rewritable displacement media, PMMA
  - Large array of independently Z-axis controlled tips
  - High data transfer rates, concurrent data transfer to/from multiple tips

Write Mechanism

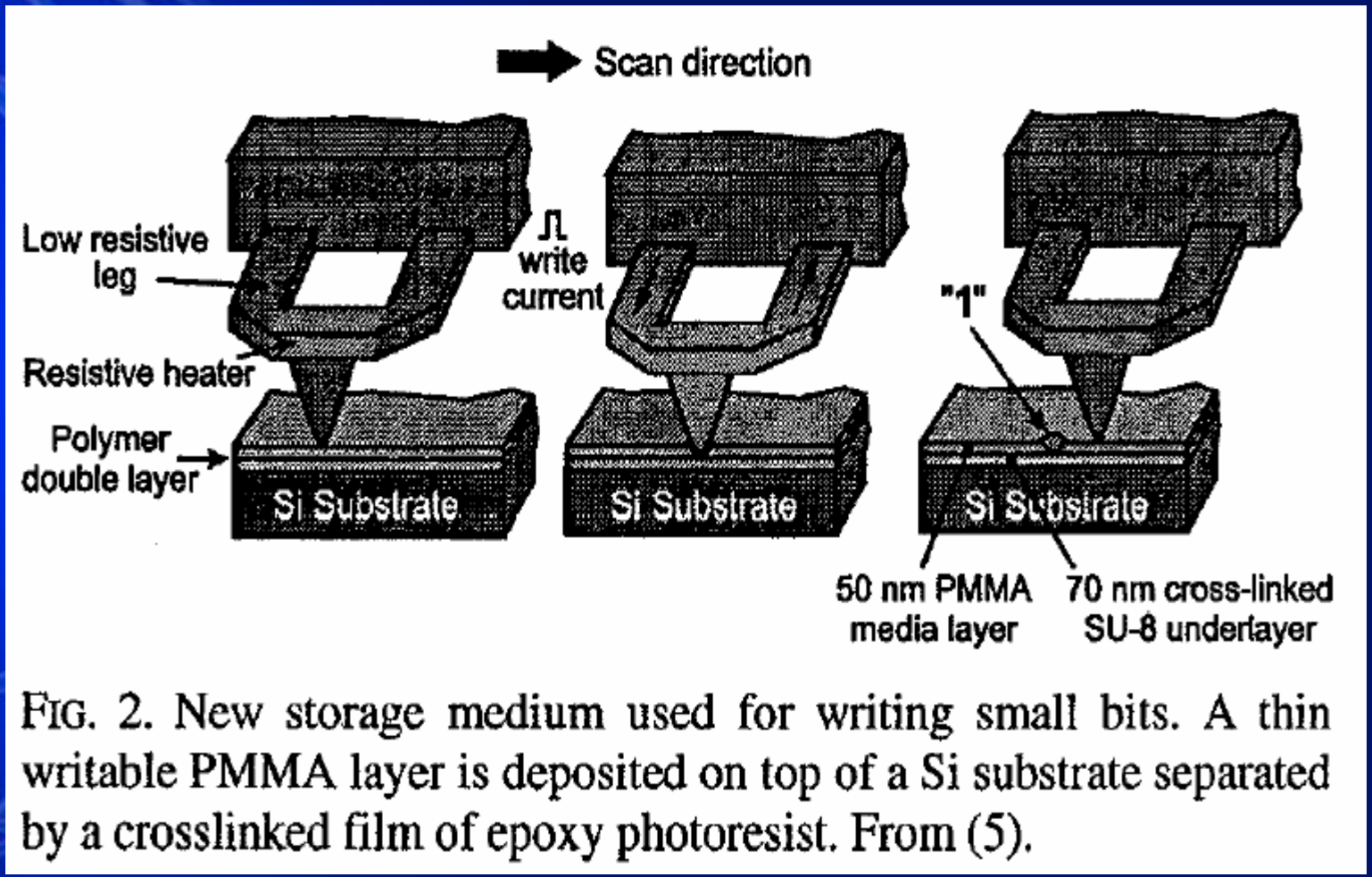


FIG. 2. New storage medium used for writing small bits. A thin writable PMMA layer is deposited on top of a Si substrate separated by a crosslinked film of epoxy photoresist. From (5).

"Thousands of Microcantilevers for Highly Parallel and Ultra-dense Data Storage", P. Vettiger et al., 2003 IEDM Technical Digest, Session 32.1.

Multiple Cantilevers

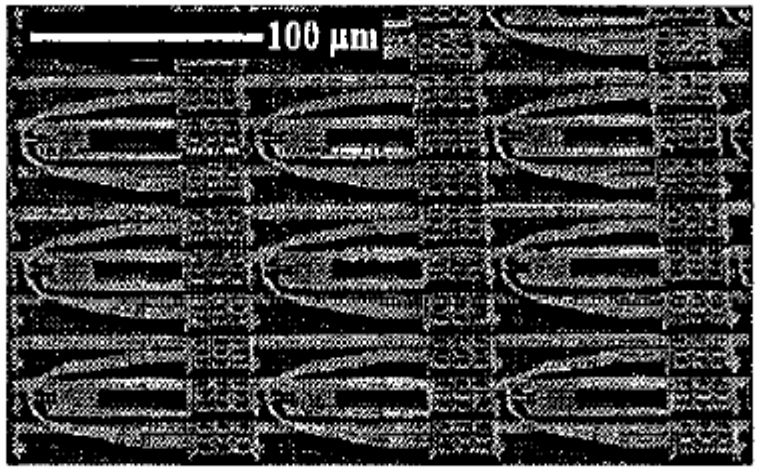


FIG. 6. SEM image of a section of the cantilever array transferred and interconnected onto its corresponding carrier wafer. From (10), © VLDB Endowment 2003.

"Thousands of Microcantilevers for Highly Parallel and Ultra-dense Data Storage", P. Vettiger et al., 2003 IEDM Technical Digest, Session 32.1.

Storage Platform

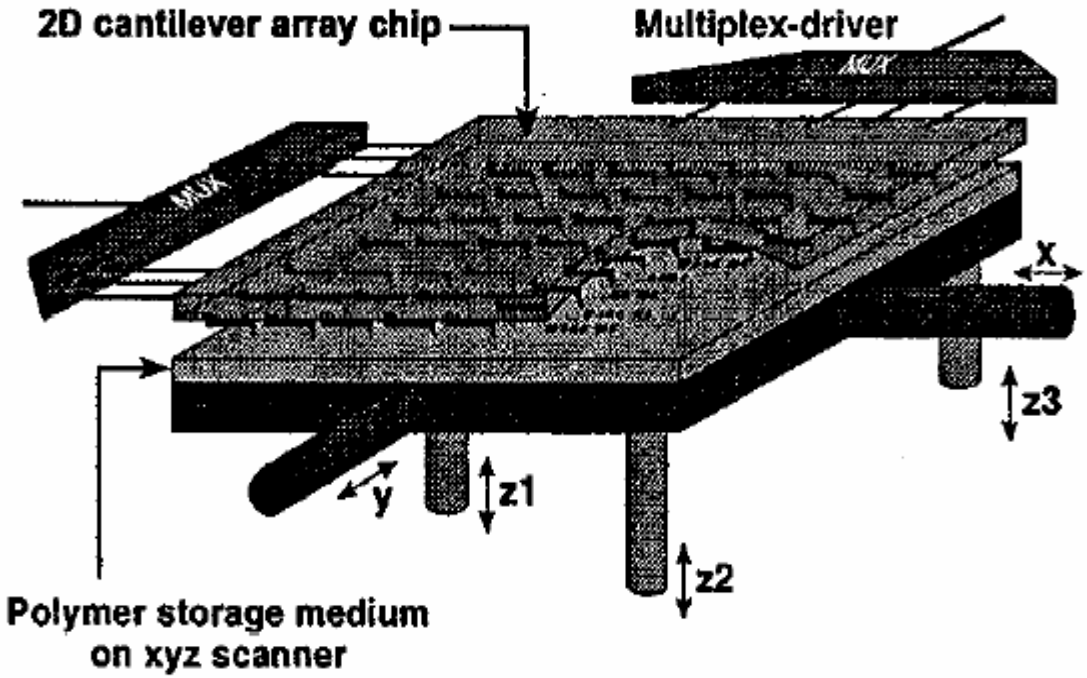


FIG. 1. The "millipede" concept. From (9).

"Thousands of Microcantilevers for Highly Parallel and Ultra-dense Data Storage", P. Vettiger et al., 2003 IEDM Technical Digest, Session 32.1.

Integrated System

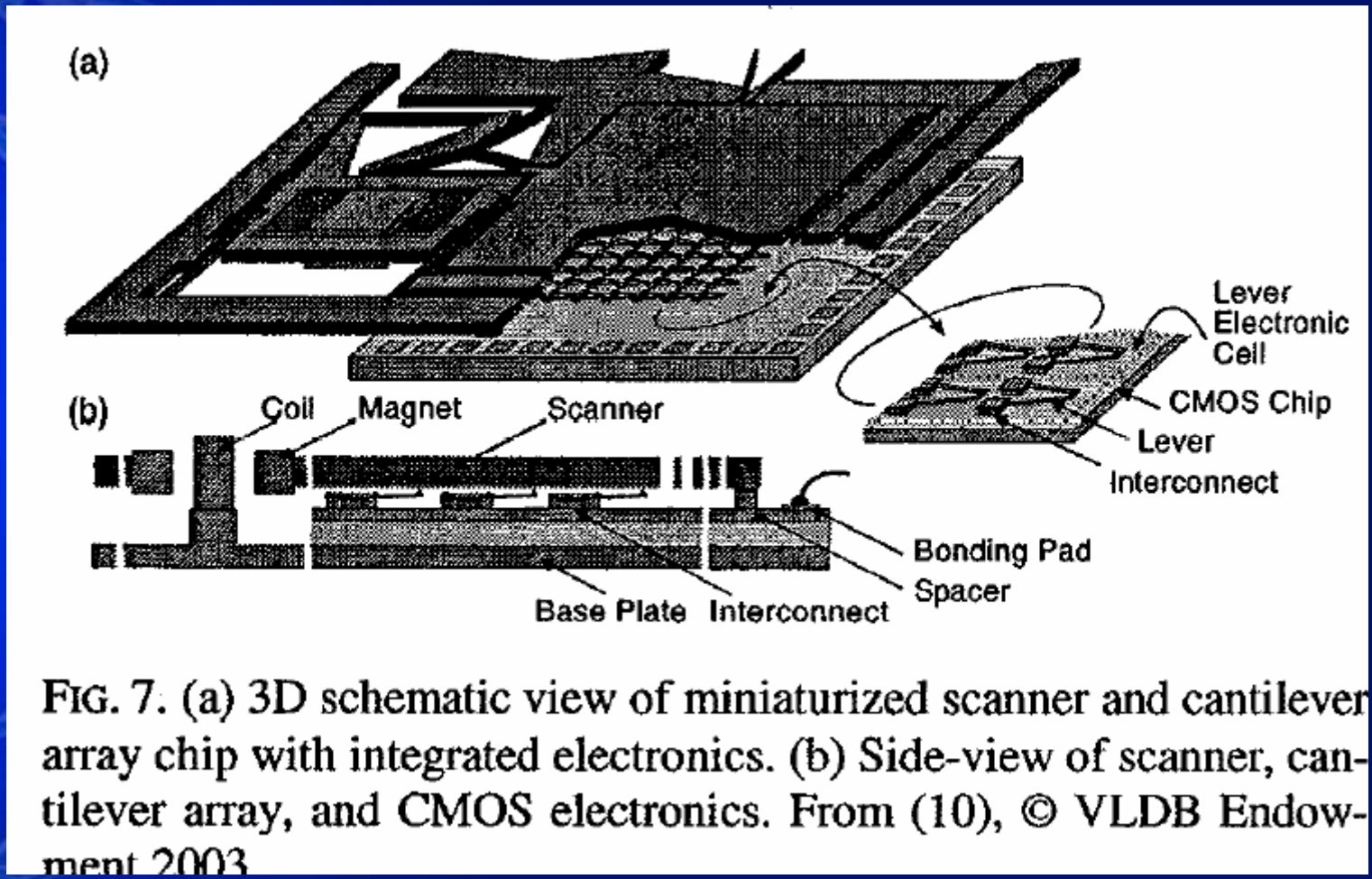


FIG. 7. (a) 3D schematic view of miniaturized scanner and cantilever array chip with integrated electronics. (b) Side-view of scanner, cantilever array, and CMOS electronics. From (10), © VLDB Endowment 2003

"Thousands of Microcantilevers for Highly Parallel and Ultra-dense Data Storage", P. Vettiger et al., 2003 IEDM Technical Digest, Session 32.1.

Storage Capability

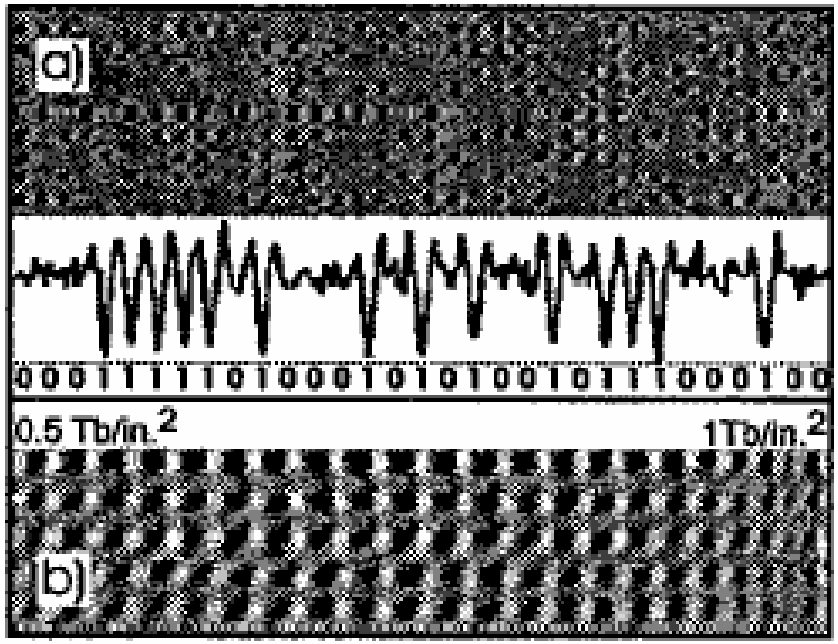


FIG. 4. (a) Data-bit section written and read back (160 Gbit/in.^{2}) by a single cantilever. (b) Data bits with areal densities approaching 1 Tbit/in^2. From (10), © VLDB Endowment 2003.

"Thousands of Microcantilevers for Highly Parallel and Ultra-dense Data Storage", P. Vettiger et al., 2003 IEDM Technical Digest, Session 32.1.

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Summary

- Moore's Law Continues: NOR and NAND high volume NV memories for the rest of the decade, scaling visibility to 32 nm node, nanocrystal scaling enabler
- Non transistor memory scaling best opportunity beyond 32 nm node
- Non litho defined memory provides opportunity to go beyond Moore's Law